Journal of Instrumentation

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To cite this article: K. Penski on behalf of the ATLAS Muon Spectrometer System collaboration 2024 *JINST* **19** C05008

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Published by IOP Publishing for Sissa Medialab

Received: *November 3, 2023*
Accepted: *February 12, 2024*
Published: *May 10, 2024*

Topical Workshop on Electronics for Particle Physics
Geremeas, Sardinia, Italy
1–6 October 2023

Test result of the new ASD2 chips for Phase-II upgrade of the ATLAS MDT chambers at HL-LHC

K. Penski on behalf of the ATLAS Muon Spectrometer System

Ludwig-Maximilians-Universität München,
Am Coulombwall 1, Garching, Germany

E-mail: K.Penski@physik.uni-muenchen.de

Abstract: For the Phase-II upgrade of the ATLAS Muon Spectrometer to High-Luminosity LHC, new front-end readout electronics for the Monitored Drift Tube chambers is required, as the old one no longer meets the demands. The first stage in the Monitored Drift Tubes readout chain is the Amplifier-Shaper-Discriminator chip. For the upgrade, the new ASD2 ASIC chip in IBM 130 nm CMOS technology has been developed. For the ATLAS experiment, 80000 ASD2 chips are produced, which have to be tested before integration in order to obtain the required 50000 well-performing chips in the end. Using a prototype tester board and pre-production ASD2 chips, the overall performance and the influence on programmable parameters is investigated. Based on these results, 1775 production chips are tested to define final optimized cut values for the automated production testing of all chips in the company.

Keywords: Front-end electronics for detector readout; Muon spectrometers

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https://doi.org/10.1088/1748-0221/19/05/C05008

Contents

1 Motivation and testing strategy

The Monitored Drift Tube (MDT) chambers [1] are part of the ATLAS Muon Spectrometer at the Large Hardron Collider (LHC) [2] and used for precise muon tracking. Due to the higher particle fluxes (up to 300 kHz/tube [3]) after the High-Luminosity LHC (HL-LHC) upgrade, the MDT's trigger and data acquisition system needs essential modification because the current front-end electronics do not meet the demands [4–6]. For the HL-LHC upgrade a new Amplifier-Shaper-Discriminator (ASD2) chip has been developed (see section 2) [3, 7], which forms the first MDT readout stage and is crucial for the MDT performance regarding time resolution, noise and efficiency [7]. The overall performance of the chip and the dependence on programmable parameters is studied using 100 pre-production ASD2 chips and a prototype tester board. The results are presented in section 3. For the Phase-II upgrade about 80000 new ASD2 chips were produced and 50000 are needed for installation. Consequently, a procedure has to be implemented in order to provide well-performing chips to ATLAS. Therefore, 1175 production chips have been tested using a newly designed tester board aiming to set and verify the testing parameters and cut intervals for the production testing. The challenge is to reject all non-working chips and achieve a high uniformity among the channels of all chips while still aiming for a sufficient yield. A final categorization principle is introduced in section 4 taking all demands into account. It is used for the production testing of the 80000 ASD2 chips in a specialized company.

2 The ASD2 chip

The new 8-channel ASD2 chip has been developed using IBM 130 nm CMOS 8RF-DM technology [3, 7]. Figure 1 shows the functionality [8, 9]. The signal is sent to a Wilkinson ADC. It encodes the signal's pulse height into the LVDS output pulse width, digitized in a separate TDC with high resolution for time-slewing correction [10]. The ADC integrates for typ. 16 ns and applies a typ. 55 ns

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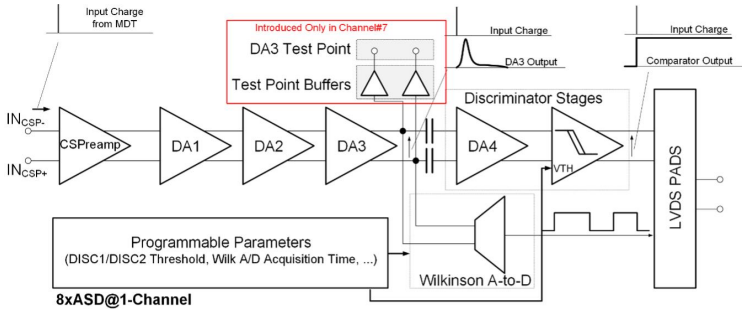

Specs / Param	Value	Bits
Sensitivtiy	8.9 mV/fC	-
Noise	ENC = 6000 e⁻ RMS	-
DISC1 Threshold	-255 to 255 mV	8
DISC1 Hysteresis	0 - 320 µA	4
WADC Integration Gate	8 - 45 ns	4
WADC Rundown Current	2.4 - 7.3 µA	3
WADC Dead Time	13.8 - 785 ns	3

Figure 1. Block diagram of one ASD2 channel: the input charge from one MDT is amplified and shaped. Different programmable parameters are set, such as the threshold and hysteresis in the discriminator stage or the rundown current (rdc) in the Wilkinson ADC (WADC). Reproduced with permission from [9].

rundown gate, leading to a conversion within 3 clock cycles of the 40 MHz LHC clock. These and other parameters like the dead time or the rundown current (rdc) are programmable and affect the chip's performance (see section 3). The table in figure 1 shows the parameters discussed here, but in total 55 bits of configuration data are sent to the ASD. The signal is sent to the LVDS PADS cell.

3 ASD2 chip characterization and functionality

100 pre-production ASD2 chips are characterized using a prototype tester board investigating the influence of the programmable parameters.

3.1 Basic health measurement

For all channels of the chip a homogeneous power supply has to be ensured. The drawn current is measured at different power domains, as shown for two of them (VDD3 and VDDA) in figure 2.

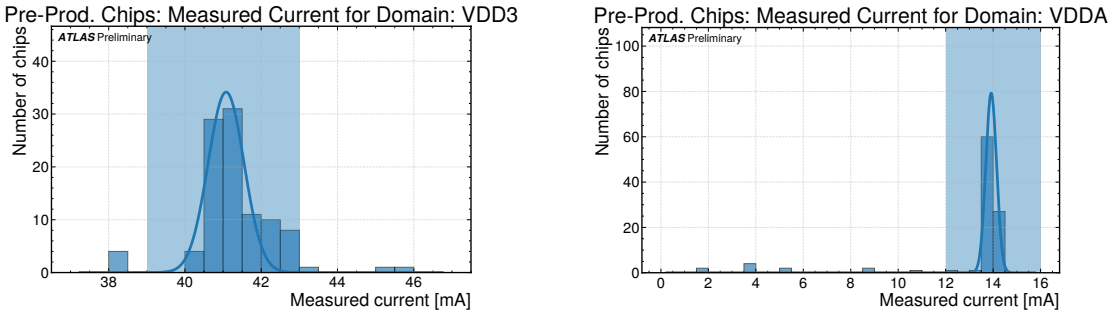

Figure 2. Measured current drawn by the power domains VDD3 (left) and VDDA (right). The blue area indicates the acceptance interval. All chips outside this interval draw an abnormal current and are rejected.

3.2 Threshold measurement

If a signal exceeds the threshold value, it is processed. Noise leads to multiple threshold crossings, which is prevented by a hysteresis value. Both values form the effective threshold value. For the measurement 100 pulses with a defined charge Q_{in} are injected in each channel, resulting in a S-curve shown in figure 3 (left). The inflection point is taken as the threshold. If the efficiency stays constant,

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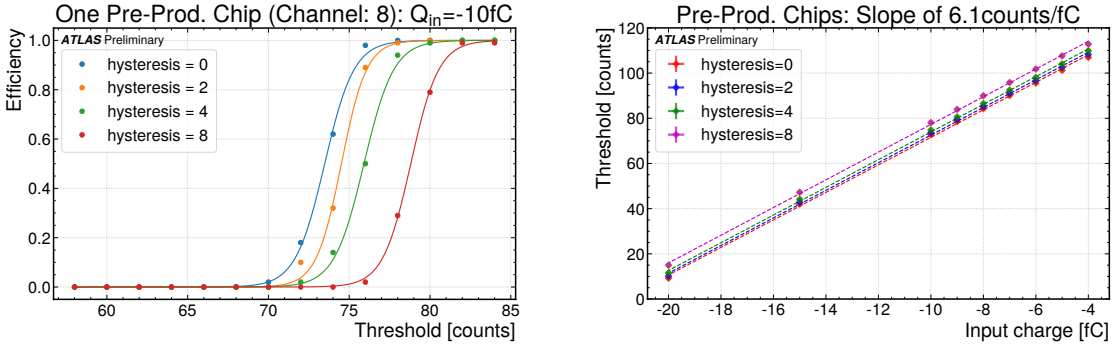

Figure 3. Left: the efficiency (ratio of detected to generated pulses) is measured as a function of the discriminator threshold value for different hysteresis values. With increasing hysteresis, the threshold shifts to larger values. Right: there is a linear correlation between the input charge and the resulting threshold value, with an offset caused by the hysteresis.

the channel is dead and the chip is rejected. This measurement is performed for various Q_{in} and the result is summarized in figure 3 (right). To be sensitive to charges around −4 fC, the corresponding threshold of 115 counts is taken. Hysteresis 8 is chosen to minimize noise effects.

3.3 Dead time measurement

A single muon track passing a MDT can cause multiple threshold crossings. By introducing a dead time for the total MDT drift time of about 700 ns after the first pulse, this effect is counteracted [9]. In the ASD chip, the dead time is implemented by the dead time code and can be measured as shown in figure 4 (left). For the resulting S-curve, the same procedure introduced in section 3.2 is used. To get the MDT dead time of at least 700 ns, a dead time code of 6 or 7 is needed (figure 4, right).

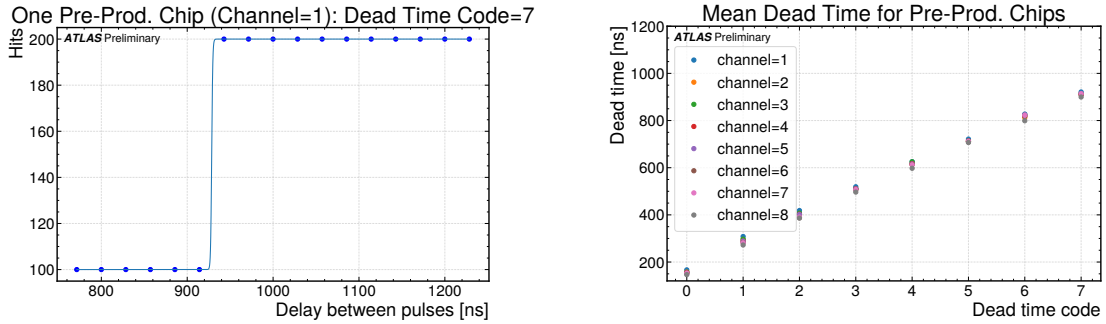

Figure 4. Left: for the dead time measurement two pulses with different delays are injected, where the number of hits is measured as a function of the delay. Right: there is a linear dependency between the mean dead time and the programmable dead time code.

3.4 Pulse width measurement

The ASD chip has to provide information about the deposited charge in the MDTs. Therefore, the signal charge is measured, which is encoded into a pulse width by the dual-slope 'Wilkinson' technique. As shown on the left plot of figure 5, there is a rather linear dependence between input charge and pulse width, which saturates for input charges larger than −40 fC. The rundown current (rdc) is a

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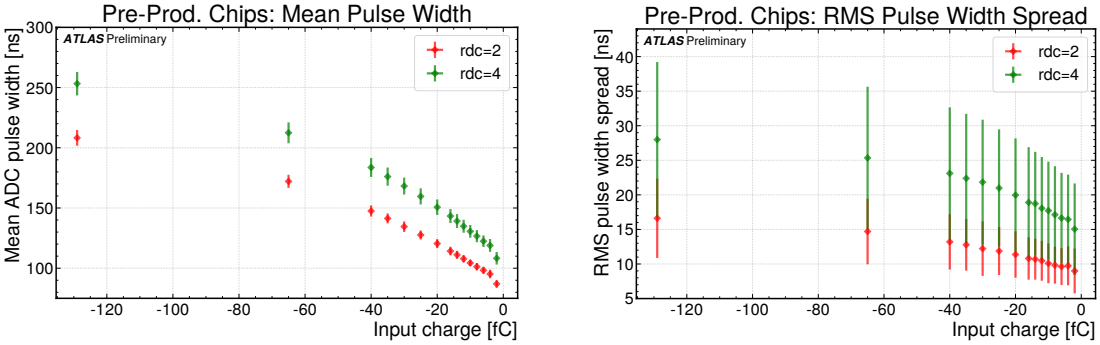

Figure 5. Left: the correlation between the mean ADC pulse width and the input charge is illustrated for two rdc. Right: the corresponding RMS pulse width spread for rdc = 4 is about twice as large as for rdc = 2.

programmable parameter defining the discharging timing of a capacitor. Since the root mean square (RMS) pulse width spread for rdc = 4 is larger than for rdc = 2 (see figure 5, right), rdc = 2 is preferable.

4 Final testing parameters and characterization

To determine the final cut intervals for production testing at the company, 1175 ASD2 production chips (identical to the pre-production chips) are tested with a new tester that is more rigidly constructed compared to the prototype to withstand the greater forces during production testing, but there is no difference in performance between the testers.

4.1 Categorization procedure

There are three categories: C (non-working chips, e.g., abnormal currents, dead channel), B (working chips, outside acceptance interval), and A (working chips, within acceptance interval). The cuts are optimized to achieve 70 % in A, which yields the number of ASD2 chips needed for ATLAS.

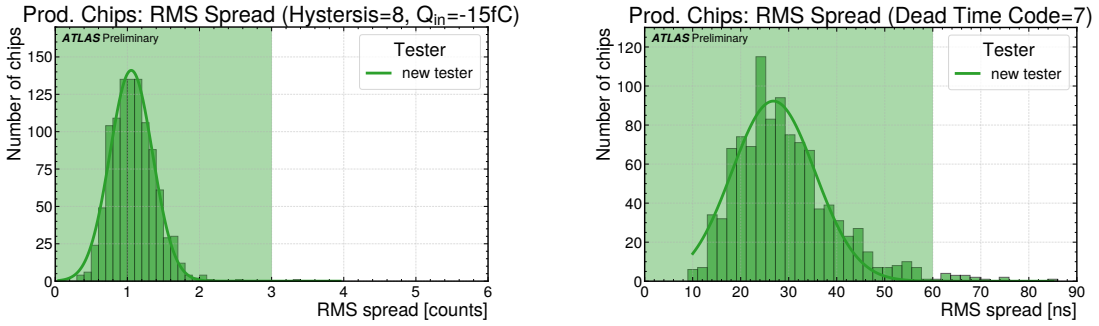

Figure 6. If the chips have spreads of < 3 counts (threshold, left) and < 50 ns (dead time, right), they belong to the acceptance interval of category A, otherwise they fall into category B.

Categorization cuts are performed for all four criteria (introduced in section 3), selected ones of which are shown in figure 6 for threshold (left) and dead time (right) and in figure 7 (left) for pulse width measurements. Since a larger rdc leads to a wider distribution (see figure 7, right), the cut values are chosen to reduce the tail of the distributions.

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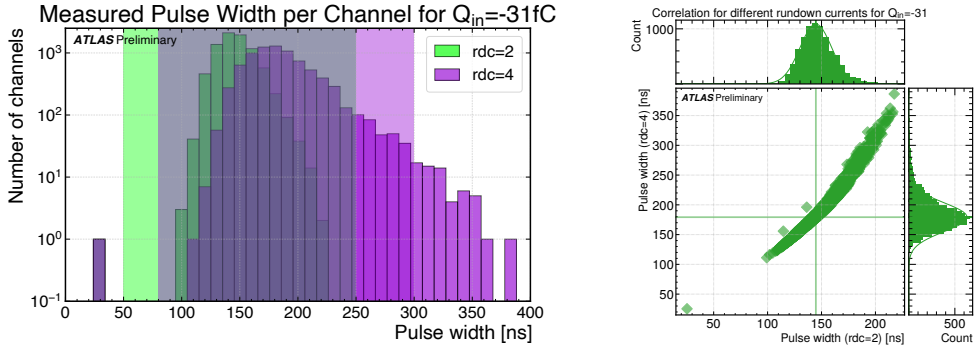

Figure 7. Left: for the pulse width measurement, distribution cuts are performed for rdc = 2 : [50, 250] ns and rdc = 4 : [80, 300] ns. Chips within the intervals belong to category A, otherwise to category B. Right: the pulse width correlation plot shows a broader distribution for larger rdc.

According to all the cuts performed in the various criteria, including additional cuts to those presented here, 14 % of the chips are in category C, 15 % in B, and 71 % in A. The target ratio for category A is achieved and only well-performing chips are included.

4.2 Basic health test verification

As shown in figure 8, the verification of the basic health cuts distinguishes between those chips that fail at a stage other than basic health and those that pass. Using category A cuts (38 mA < I_{VDD3} < 44 mA and 12 mA < I_{VDDA} < 16 mA), only chips that would fail in a later stage are rejected. If they are even further away from this interval, they are put directly into category C. However, this justifies the cuts in the basic health test, since they only select non-working chips.

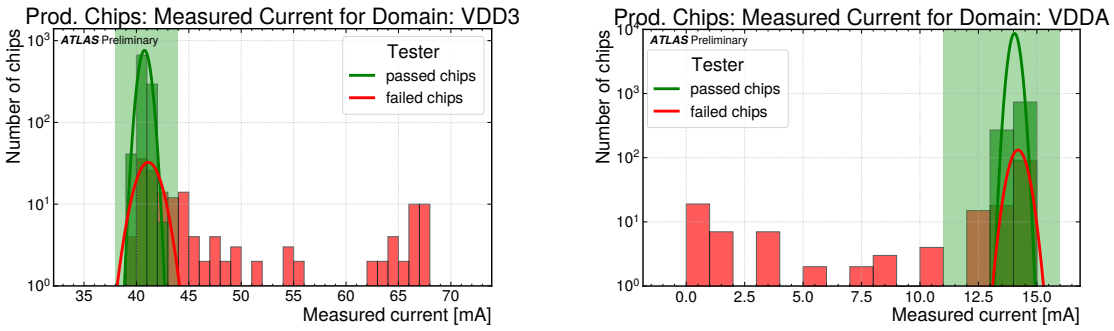

Figure 8. To justify the basic health cuts, chips that fail any criteria other than basic health are marked in red, while those that pass all criteria are green. The highlighted area is the acceptance interval for category A. For VDD3 (left) and VDDA (right), only chips that fail a later testing stage, are rejected by the health cuts.

5 Conclusion

For the HL-LHC, the MDT readout electronics is upgraded, for which a new ASD2 chips has been developed. Before the approximately 50000 new ASD2 chips are integrated into ATLAS, they have to be tested for full functionality. In order to provide only the best performing chips to ATLAS, a testing procedure has to be implemented, which is presented in this article. Therefore, the various

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programmable parameters have been successfully investigated for the performance of the chip. For testing, a threshold value of 115 counts, which corresponds to a charge of about −4 fC, is needed to detect small charges and a hysteresis value of 8 to eliminate noise effects. To realize the dead time of 700 ns, a dead time code of 6 or 7 is desirable. For accurate encoding of the input charge, a rundown current of 2 should be selected. After setting these parameters, additional cuts are introduced to categorize the chips. They are optimized to reject all non-working chips and achieve high uniformity of the performance of all channels of all chips, while maintaining a yield of 70 % for the best chips. These verified cuts are used for the ASD2 chip production testing in the company where a test cycle took less than 15 s to complete.

Acknowledgments

We acknowledge the support of BMBF and MPG, Germany.

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