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Review

# Nanostructured Inorganic Solar Cells

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**Abstract.** Recent progress in the development of nanostructured inorganic solar cells is reviewed. Nanostructuring of inorganic solar cells offers the possibility of reducing the cost of photovoltaics by allowing smaller amounts of lower-grade photovoltaic semiconductors to be used. Various fabrication methods used to nanostructure traditional photovoltaic semiconductors are detailed and the performance of resulting devices is discussed. The synthesis of solar cells by solution-based methods using less traditional, abundant materials is identified as a promising route to widescale photovoltaic electricity generation, and nanostructured solar cell geometries are highlighted as essential in this approach. Templating and self-assembling methods used to produce appropriate low-cost nanostructures from solutions are detailed, and the performance of preliminary ultra-low-cost cells made with these structures is reviewed.

**Keywords.** Photovoltaic, nanostructured, inorganic.

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## 1 Why Nanostructure? An Introduction to the Topic

It has been predicted that the world's annual energy consumption will grow from its 2009 level of around 15 terawatt-years (TWyr) to as much as 30 TWyr by 2050 [1, 2]. With more than 100,000 TW of solar power striking the earth at anytime, photovoltaic technology has long been regarded as an integral part of the solution to the world's energy problems [2, 3]. Yet, the high cost of traditional photovoltaic technologies has prevented them from displacing a meaningful fraction of the electricity we derive from fossil fuel sources. Fortunately, the prospects for inexpensive photovoltaic electricity generation are improving. In recent years much research has focused on reducing the price, or *cost per watt*, of photovoltaic cells. In particular, the emergence of fabrication and characterization techniques on the nanometer scale (nanotechnology) has enabled new strategies to harness the sun's power in a cost-effective way.

In this review, the manner in which nanotechnology is being used to improve the cost-performance balance of photovoltaic cells composed of inorganic semiconductors will be discussed. The basics of solar cell operation will be briefly explained and traditional solar cells composed of expensive, highly-crystalline inorganic semiconductors will be summarized. Next, we will explain how controlling the morphology of the semiconductors on the scale of hundreds of nanometres or less can improve the collection of electricity-generating charges from the cells, reducing their stringent materials requirements and permitting cheaper fabrication. Various techniques for fabricating nanostructures of traditional photovoltaic semiconductors will be detailed and the performance of state of the art nanostructured inorganic solar cells will be reported. A discussion will follow, in which the availability of traditional photovoltaic semiconductors and the methods for producing relevant nanostructures will be evaluated in the context of whether truly inexpensive solar cells can be achieved. More abundant photovoltaic materials and inexpensive solution-based synthesis will be identified as promising alternatives, and nanostructuring of these abundant semiconductors will again be highlighted as essential. Current work on such *ultra-low-cost* solar cells will be summarized, highlighting fabrication techniques and their performance to date.

### 1.1 Solar Cell Basics

#### 1.1.1 How a Solar Cell Works

In photovoltaic energy conversion, an incident photon imparts energy to an electron in an absorbing material, promoting the electron to an excited state. Traditionally this has consisted of an electron being excited from the valence band to the conduction band in a semiconductor with a bandgap in the visible spectrum, leaving behind a positively-charged vacant state (hole). A solar cell usually contains an interface between electron-conducting (n-type) and hole-conducting (p-type) materials, as illustrated in Figure 1. The asymmetric junction separates the excited electrons and holes and collects them at opposite electrodes of the device, producing a voltage that can power an external circuit. If for example, a photon is absorbed in the p-type material, a majority carrier hole is conducted through the p-type layer to a collection electrode, while an electron is transported through the p-type layer to the p-n interface as a minority carrier, then through the n-type layer as a ma-

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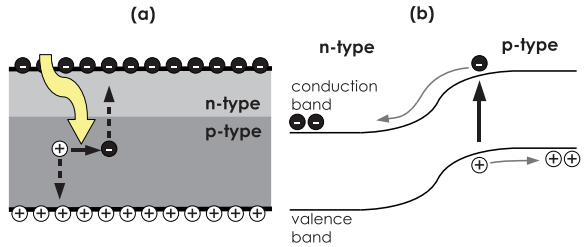


**Figure 1.** (a) Schematic cross-section of a traditional inorganic solar cell. A light-absorbing p-n junction is located between charge-collecting electrodes. (b) Band diagram of the solar cell. An electron is excited from the valence band to the conduction band by incident light, then electrons and holes are separated by the p-n junction. Charges are transported to collection electrodes as majority holes and minority electrons in the p-type layer and majority electrons and minority holes in the n-type layer.

jority carrier. The reverse is true for absorption in the n-type layer.

The absorptive and charge transport properties of the semiconductors are inextricably linked in photovoltaic cells. The semiconducting layers must be suitably thick to absorb the majority of incident radiation and must be capable of transporting the electrons and holes to the collection electrodes before they recombine. There are a number of processes through which photogenerated electrons and holes can recombine in semiconductors. These include radiative and Auger recombination, as well as Shockley Read Hall recombination at charge trap states resulting from material imperfections such as crystal defects, grain boundaries, and impurities [4]. Recombined carriers do not contribute to electricity production, and hence lower the power output of the cell.

#### 1.1.2 Traditional Solar Cell Materials

As of 2007, crystalline silicon (c-Si) cells comprised approximately 90 % of photovoltaic modules sold [5]. The performance of these cells is impressive: power conversion efficiencies (PCEs) of approximately 25 % have been obtained for monocrystalline Si cells, meaning that a quarter of all incident solar energy is converted to electrical energy [3, 6]. Meanwhile, multicrystalline Si cells have demonstrated efficiencies of more than 20 % [3, 6].

Amorphous, nanocrystalline, and thin-film polycrystalline silicon solar cells are all alternatives to c-Si, but they are hampered to varying degrees by slow deposition rates, poor stability, and inferior efficiencies [7]. Beyond c-Si, amorphous Si cells dominate the remainder of the solar cell market, primarily due to their ability to be fabricated by roll-to-roll processing on flexible substrates.

III-V compound semiconductors such as GaAs have also received much attention as solar cells. They have high reported efficiencies (greater than 26 % for crystalline GaAs [6]) due to strong absorption, but are more costly than silicon so occupy little market share. Thin-film CdTe and Cu(In,Ga)$Se_2$ heterojunction solar cells have demonstrated efficiencies of approximately 17 % and 20 % respectively, despite the polycrystalline nature of the absorbing layers [3, 6, 8].

### 1.2 The High Price of Low Carbon Emissions

In recent years, photovoltaic manufacturing has been growing at a rate of around 30 % annually [3, 5, 9].This figure appears encouraging but as of 2003, solar energy production was still only about 0.1 % of that generated by fossil fuels [5]. The stumbling block for true wide-scale implementation of solar cells to date has been their cost. The present cost of photovoltaic-generated electricity is in the range of \$0.20 to \$0.35/kilowatt-hours (kWh), as compared with the cost of coal-based electricity, which is closer to \$0.04/kWh [9]. So why is electricity produced from photovoltaics so expensive?

Consider monocrystalline silicon solar cells, which are traditionally fabricated by cutting a wafer from a single-crystal p-type ingot, doping its top surface n-type to create a p-n junction as shown in Figure 1, then applying suitable dantireflection coatings and contact electrodes. The single-crystal ingots are often produced by the Czochralski process, whereby a seed crystal is slowly extracted from a melt of high-purity silicon. Production of the high-purity silicon, the high-temperature crystal growth, and subsequent vacuum methods used for doping and contact application are all energy-intensive techniques, which result in a solar cell with a large amount of embodied energy and a high cost. This prompts an obvious follow-up question: is a fabrication method with such high energy requirements really necessary?

Returning to Figure 1, we see that for a high-efficiency solar cell, the photogenerated carriers need to be transported distances similar to the thickness of the material required for complete light absorption. In other words the recombination rate of photogenerated carriers in the semiconductor(s) needs to be low. Charge transport lengths are generally highest (recombination rates lowest) in uniform, crystalline materials free from defects, impurities, and grain boundaries. Monocrystalline silicon, for example, is capable of transporting photogenerated minority carriers well over a hundred microns [4]. Unfortunately, expensive, high temperature, vacuum-based processing methods are typically necessary to produce semiconductors of suitable crystallinity. If less crystalline semiconductors produced by less expensive methods are employed, shorter transport distances result which necessitate thinner absorbing layers that do not harvest all of the incident light, thus compromising efficiency for lower initial cost. Depending on the relative

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cost and efficiency reductions, the cost per watt of electricity produced by the cell may in fact be increased.

In 2007, Slaoui and Collins noted that even if the price of traditional silicon-based photovoltaics continued to drop at its current rate, these cells would still not be competitive enough in 40 years to constitute a significant fraction of the 30 TWyr demand [5]. III-V compound semiconductor solar cells such as GaAs are typically fabricated on single crystal substrates using epitaxial deposition and are therefore particularly expensive to make [5]. Thin film CdTe and Cu(In,Ga)$Se_2$ solar cells have been made by different growth methods, including inexpensive electrochemical deposition, and therefore have been projected to meet the U.S. Department of Energy goal of \$0.10/kWh by 2015 [8]. However, for the best performance CdTe and Cu(In,Ga)$Se_2$ cells, high-temperature processing, specifically deposition and annealing at around 500°C, is required. These cells also contain extremely rare and toxic metals, however, appropriate recycling schemes have been developed to address the toxic components [10]. Thus while implementation may be limited to certain applications where the life-cycle of the cells can be monitored, CdTe and Cu(In,Ga)$Se_2$ modules are expected to increase their market share in coming years due to their lower costs.

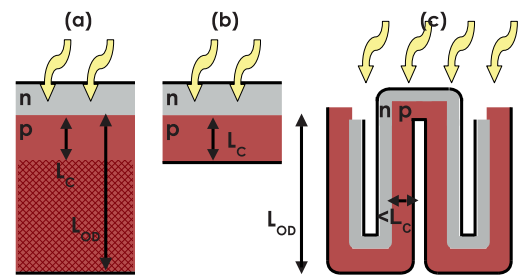


**Figure 2.** Poor charge transport limits the efficiency of solar cells made using inexpensive semiconductors. (a) The collection length $L_C$ of minority carriers in the absorbing layer is much less than the optical depth $L_{OD}$ (defined here as the thickness required to absorb 90 % of radiation with energy greater than the bandgap of the semiconductor) such that many photogenerated charges recombine before they can be removed from the cell. (b) Reducing the thickness of the absorbing layer improves charge collection but limits absorption and hence the power produced. (c) Absorption and charge collection can be decoupled into orthogonal directions by folding the semiconducting layers. In this figure it has been assumed that the n-type semiconductor is a transparent, window layer, however the same discrepancy between $L_{OD}$ and $L_C$ applies when it is absorbing.

### 1.3 Using Nanostructures to Make Inexpensive Cells More Efficient

The U.S. Department of Energy has set an ultimate cost goal of \$0.05 to \$0.06/kWh for utility-scale photovoltaic electricity production. Albeit a lofty goal, researchers around the globe are addressing this problem through intensive research into a wide variety of photovoltaic materials and structures [3]. In recent years, photovoltaic materials have been nanostructured in an effort to simultaneously achieve high efficiencies and low cost, by reconciling short transport distances with thick absorbing layers. Figure 2 (a) displays a solar cell whose performance is limited by poor carrier transport. It could, for example, consist of polycrystalline semiconductors fabricated using inexpensive techniques. The optical depth $L_{OD}$ of the absorbing layer (defined here as the thickness required to absorb 90 % of radiation with energy greater than the bandgap of the semiconductor) is much larger than the charge collection length $L_C$ in the device. While the majority of incident light is absorbed by the cell in Figure 2 (a), photogenerated minority carriers created at distances greater than $L_C$ from the p-n junction recombine before reaching the interface and do not produce electrical power. Also, the thick p-type layer may inhibit the flow of majority holes to their collection electrode, further reducing the power conversion efficiency. If the thickness of the absorbing layer is instead limited to the minority carrier collection length, as shown in Figure 2 (b), photogenerated electrons and holes are collected much more efficiently, but the amount of light absorbed, and hence the efficiency of the solar cell remains low.

In Figure 2 (c), a thin solar cell has been folded to increase its effective absorbing thickness. In doing so, the absorption and charge collection functions are decoupled into orthogonal directions. The semiconducting layers are still thin enough that photogenerated charges can be efficiently transported out of the cell, while the overall cell thickness is sufficient to absorb all incident radiation.

Figure 3 displays various methods by which this folded architecture can be achieved. In Figure 3 (a) the various layers are coated onto a supporting nanostructure. Alternatively, the semiconductors can be directly nanostructured, as is illustrated in Figure 3 (b) and (c). In (b) a radial p-n junction is formed by coating a semiconducting layer onto an array of semiconducting nanorods or nanowires. In (c), such an array has been filled with a complementary semiconductor.

For the coated architecture in Figure 3 (a), short transport distances $< L_C$ result for both the transport of photogenerated minority carriers to the interface and for the transport of majority carries to both electrodes. Conversely, in the filled nanostructure of Figure 3 (c), the greater separation between collection electrodes means that while a short transport distance is created for minority carriers traveling to the p-n interface, majority carriers have a larger distance to be transported to the collection electrodes. As it is the minority carrier transport length that typically limits

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charge collection from inorganic solar cells, both architectures can provide considerable performance enhancements. However, depending on the specific material properties and required cell thickness, majority carrier transport can be a limiting factor. In the radial p-n junction architecture of Figure 3 (b), short transport distances are provided for majority carriers through one semiconductor, while a longer distance exists in the nanowire array. Thus an appropriate nanostructure can be selected, based on ease of synthesis and relevant semiconductor properties.

By using appropriate nanostructures, the stringent material requirements for photovoltaic semiconductors can be relaxed, leading to potential cost reductions. In the case of crystalline silicon for example, it has been reported that a third or more of the total energy requirement for the fabrication of photovoltaic modules is attributable to the purification of metallurgical grade silicon to solar grade [11]. Such nanostructures can also reduce lattice matching requirements for heterojunctions due to strain accommodation at the nanowire surfaces, their inorganic materials have better proven stability than other low-cost technologies such as organic and dye-sensitized solar cells [12–15], and they can also improve light absorption, permitting the use of thinner absorbing layers.

## 2 Nanostructuring of Traditional Inorganic Solar Cells

### 2.1 Fabrication Methods

In this section, we summarize some of the methods that have been employed to nanostructure traditional photovoltaic semiconductors into the forms shown in Figure 3. In particular, arrays of nanorods or nanowires (NWs) have been synthesized using vapor deposition techniques based on a vapour-liquid-solid (VLS) mechanism, by etching of stock materials, and by template-assisted methods.

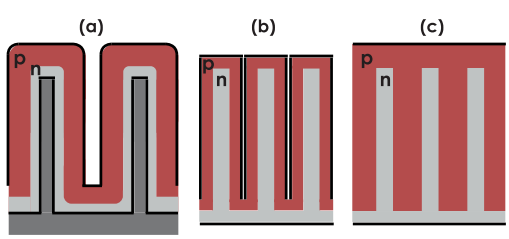


**Figure 3.** Folded nanostructures that decouple absorption and minority carrier transport can be achieved by (a) coating the layers onto a supporting nanostructure or (b-c) directly structuring the p-n junction. (b) A radial p-n junction formed by coating a complementary semiconductor onto an array of nanorods or nanowires. (c) A nanorod or nanowire array filled with a complementary semiconductor.

#### 2.1.1 Vapor-Liquid-Solid Techniques

In the VLS method [16], a catalyst material such as gold, iron, silver, copper or nickel is melted on a substrate to form liquid droplets, as shown in Figure 4 (a). A precursor gas is then introduced and the desired species is absorbed by the droplet. When supersaturated, the species precipitates from the droplet, forming a crystalline solid at the droplet-substrate interface, as shown in Figure 4 (b). As this process continues, the droplet is displaced from the substrate and a crystalline nanowire is formed, as shown in Figure 4 (c). The growth continues until the catalyst is consumed (catalyst impurities are incorporated into the growing nanowire) or the growth conditions are changed. The nanowire diameter has been shown to depend on the size of the catalyst droplet [17] as well as reaction parameters such as temperature and precursor pressure [18, 19]. Crystalline nanowires of a variety of relevant semiconductors such as Si, Ge, GaAs, CdS and CdSe with diameters down to a few nanometres and lengths greater than 75 μm have been produced [16–27].

Figure 5 (a) displays a disordered array of Si NWs formed by VLS growth on a silicon substrate [26]. VLS NWs have been grown on a variety of substrates such as monocrystalline silicon [25, 26], multicrystalline silicon on glass [26], single-crystal GaAs [27], and stainless steel [25]. Vertically-aligned NW arrays can result with suitable growth conditions and epitaxial matching between the substrate and wires. Figure 5 (b) displays an array of vertically aligned GaAs NWs formed on a GaAs substrate [27]. Although the GaAs wires form vertically to the substrate, the spacing between adjacent wires is seen to vary. VLS growth can be combined with patterning of the catalyst material to control the diameter, spacing, and arrangement of the nanowires [23, 28]. Figure 5 (c) displays an ordered Si NW array grown by a VLS technique where a photolithography method was used to order and confine the liquid metal catalysts [23].

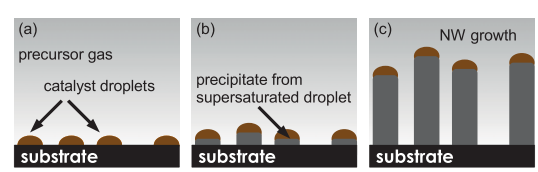


**Figure 4.** Vapor-liquid-solid growth mechanism. (a) Catalysts particles are melted on an appropriate substrate and a suitable precursor gas introduced. (b) Liquid droplets become supersaturated with desired NW material and form a precipitate at the liquid-substrate interface. (c) Precipitation continues, resulting in NW formation and growth until the deposition conditions are adjusted.

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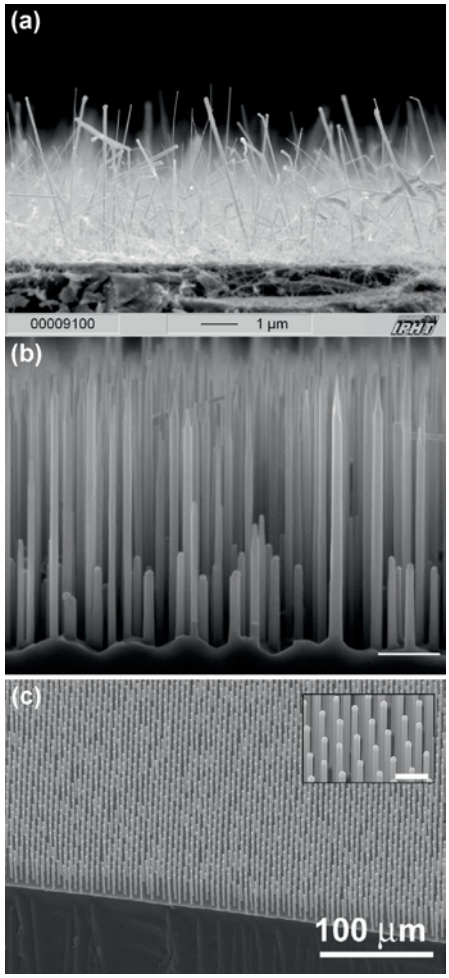


**Figure 5.** Various NW arrays grown by VLS methods. (a) Disordered array of n-type Si NWs grown on a silicon substrate. (Reprinted with permission from [26]. Copyright 2008 Institute of Physics.) (b) Vertically-aligned GaAs NWs grown on a GaAs substrate. Radial NW growth permitted p-n junction formation by introducing appropriate dopants throughout the deposition. Scale bar is 500 nm. (Reprinted with permission from [27]. Copyright 2009 American Chemical Society.) (c) Perfectly ordered Si NW array formed by patterning metal catalysts via photolithography. (Reprinted with permission from [23]. Copyright 2007 American Institute of Physics.)

### 2.1.2 Metal-Catalyzed Electroless Etching of Silicon Substrates

Metal-catalyzed electroless etching (MCEE) has been used to produce large area arrays of Si NWs on both monocrystalline and polycrystalline silicon substrates. It is based on the metal-induced local oxidation and dissolution of silicon in aqueous hydrofluoric acid (HF) solutions. Metallic atoms deposited on the substrate behave as a cathode, inducing further deposition of metallic dendrites, while the area surrounding these nuclei behaves as an anode and is etched away in the solution, as illustrated in Figure 6 (a) [29, 31–34]. The morphology of the nanowires can be influenced by varying the type and concentration of the metal species, the temperature of the etching solution, as well as the etching time. The crystallographic orientation of the wires is determined by that of the substrate. Wires with diameters of 20–150 nm and lengths of 10–50 µm have typically been produced. Figure 6 (b) displays a SEM cross-section of a Si NW array selectively etched from a p-type Si(111) substrate [29].

In different etching solutions, the Si substrate can instead be dissolved at the location of the deposited Ag species, as shown in Figure 6 (c) [30, 35]. Similar nanowire lengths and diameters can be produced. In work by Fang et al., slanted NW arrays were created, which was attributed to anisotropic etching of the Si underneath the metal clusters, and to competition between different etching directions [30]. Figure 6 (d) displays a SEM cross-section of a slantingly-aligned Si NW array created by MCEE of a Si substrate in a $HF/H_2O_2/H_2O$ solution [30]. Recently, Peng

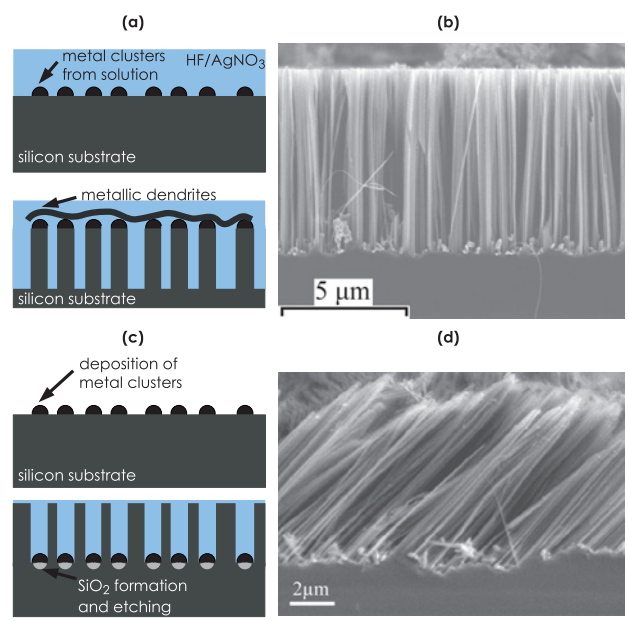


**Figure 6.** (a) Mechanism of metal-catalyzed electroless etching (MCEE) of NWs from a silicon substrate. Metallic atoms deposited from an ionic metal HF solution facilitate dissolution of the surrounding silicon. (b) p-type Si NW array etched from a monocrystalline substrate in a $HF/AgNO_3$ solution [29]. (Copyright Wiley-VCH Verlag GmbH & Co. KGaA., Reproduced with permission.) (c) Alternative MCEE method where etching occurs underneath deposited Ag particles. (d) Slantingly-aligned Si NW array fabricated by anisotropic etching underneath metal clusters. (Reprinted with permission from [30]. Copyright 2008 Institute of Physics.)

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et al. patterned the Ag catalyst with UV lithography before selectively etching to produce ordered nanohole arrays in silicon substrates [36]. Such nanohole geometries have the advantage of greater mechanical stability than freestanding nanowire arrays.

### 2.1.3 Template-Assisted Synthesis

Suitable nanostructures have also been fabricated using templating methods. A variety of nanoscale templates with vertically-aligned pores have been developed, which can either be filled with an appropriate semiconductor or used as masks for patterning underlying semiconductor layers. Relevant templates include self-assembling monolayers of nanoscale materials [37,39], anodic aluminum oxide (AAO) templates [40–43], and block copolymers [44, 45].

Garnett and Yang constructed templates by dipcoating n-type silicon substrates in solutions of silica beads [37]. The beads formed self-assembling monolayers on the substrate surface, as shown in Figure 7 (a). The underlying silicon was then patterned using deep reactive ion etching (DRIE), resulting in the nanowire structures shown in Figure 7 (b). The NW spacing and diameter can be controlled by the size of the silica beads and the NW length by the etch time. The NWs produced in their work were typically 390 nm in diameter and 5 μm long.

Anodic aluminum oxide (AAO) was introduced as a self-organizing mesoporous structure by Keller et al. in 1953 [40]. It is prepared by anodically oxidizing an aluminum foil or film in an acidic solution under a constant voltage. Surface curvature at cracks and other depressions in the oxide surface results in an enhanced local field, which accelerates the oxide formation and dissolution rates, resulting in the formation of vertically-aligned, nano-sized pores. The pores can then be filled with relevant semiconductors, as shown in Figure 7 (c), by methods such as pressure injection, electrochemical deposition, and capillary filling with sol-gels [43, 46]. Both the spacing and diameter of the pores, and hence of the nanostructures, can be controlled via the anodization conditions. Pores can be produced with diameters ranging from 10 to 200 nm, lengths over 100 μm, and pore spacings ranging from 10 nm to over 400 nm [46, 47]. The diameter of the pores can be further adjusted following anodization via a pore-widening step, where a 5 wt % phosphoric acid solution is generally used [48, 49].

Fan et al. fabricated nanostructured CdS-CdTe solar cells using CdS nanopillar arrays synthesized in AAO templates [38]. Highly regular templates approximately 2 μm thick with pore diameters of approximately 200 nm were formed on Al foil. Approximately 300 nm of Au was electrodeposited at the bottom of the pores and single-crystal CdS nanowires were grown by a VLS method. The templates were then selectively etched to expose the CdS nanopillars, as shown in Figure 7 (d).

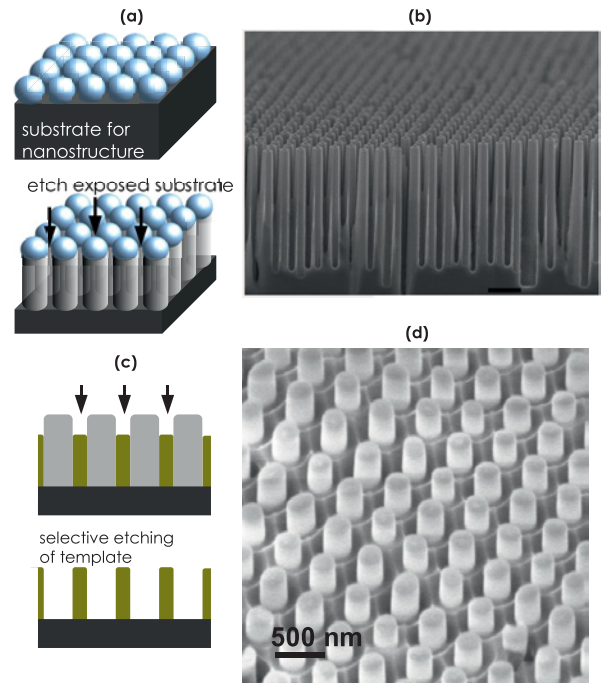


**Figure 7.** (a) Nanostructure synthesis using self-assembling monolayer templates. An underlying substrate is patterned through the template to produce a replicate nanostructure. (b) n-type Si NW array synthesized by deep reactive ion etching through a self-assembling monolayer of silica beads. Scalebar is 1 μm. (Reprinted with permission from [37]. Copyright 2010 American Chemical Society.) (c) Nanostructure formation via filling then removal of self-assembling anodic alumina templates. (d) Vertically-aligned CdS nanopillar array synthesized on Al foil substrate by VLS deposition into an anodic alumina template. (Reprinted by permission from Macmillan Publishers Ltd: Nature Materials [38], copyright 2009.)

### 2.1.4 Cell Fabrication

For a photovoltaic cell, a p-n junction is desired. In the case of the GaAs VLS NWs shown in Figure 5 (b), the deposition conditions result in both axial and radial growth, such that radial p-n junctions can be created simply by introducing p-type and n-type dopants throughout the deposition [27,50]. For other NW growth conditions and methods, where it is predominantly axial growth that results, radial p-n junctions have been formed by depositing a complementary semiconductor layer after NW growth by techniques such as chemical vapor deposition (CVD) [24, 25, 34], as illustrated schematically in Figure 8 (a). Annealing is often required to improve the crystallinity of the deposited layer. Figure 8 (d) shows a TEM image of a radial p-n junction formed by depositing a p-type amorphous Si shell by liquid phase CVD onto n-type single crystal NWs produced by MCEE [34]. Cores 50–100 nm in diameter were pro-

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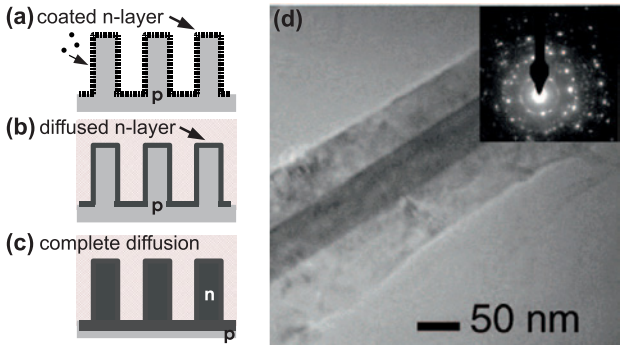


**Figure 8.** Various techniques for p-n junction formation on NW arrays. (a) Conformal coating of complementary semiconductor. (b) Diffusion doping of NW array. (c) Extended diffusion doping creates a planar junction. (d) TEM image of a radial Si p-n junction. The polycrystalline p-Si shell was formed by CVD and annealing. The single-crystal n-Si NW core was synthesized by selective etching. The selected area electron diffraction pattern of the wire is shown in the inset. (Reprinted with permission from [34]. Copyright 2008 American Chemical Society.)

duced with shells around 150 nm in thickness, which required rapid thermal annealing at 1000 °C for 10 s to convert them from amorphous to polycrystalline. Alternatively, the space in between the nanowires can be completely filled by techniques such as CVD or electrochemical deposition, to form a nanostructured p-n junction with an architecture like that shown in Figure 3 (c). The CdS nanopillar array in Figure 7 (d) for example, was completely filled by a 1 µm thick CdTe film deposited by CVD [38].

NWs can also be diffusion doped to produce junctions [29, 30, 37]. The NW array is annealed in an appropriate gaseous environment, such that diffusion of dopant species into the exterior of the NWs occurs, resulting in the architecture shown in Figure 8 (b). However, for thin NWs or long diffusion times, doping of the entire NW can result, as shown in Figure 8 (c), such that a planar p-n junction is formed at the base of the NWs rather than radially along the NW length. In such cases, a nanostructured antireflective coating (ARC) is formed, rather than a nanostructured p-n junction [29, 30].

In the case of NWs grown by VLS, MCEE, or templating methods, appropriate etching steps are required to remove the metal catalysts or templates, typically before junction formation. Appropriate etching routines are also sometimes required to remove amorphous or oxide layers from the outside of the nanowires before device fabrication.

Front and back contacts are then applied by techniques such as sputtering, evaporation, or the lamination of a polymer foil with a transparent conducting oxide layer. It is important that continuous collection electrodes are formed, which can be difficult to achieve in nanostructured cells with porous architectures like those illustrated in Figure 3 (a) and (b). For contacts deposited by physical vapor methods, the contact material often does not completely fill the space between the wires or coat the entire length of the wires, such that discontinuities result. Fang et al. found that more continuous and compact electrodes could be applied on slanted NW architectures than on vertically-aligned arrays, reducing the parasitic cell resistance [30]. Porous nanostructured architectures often additionally necessitate appropriate masking techniques to ensure that each collection electrode only contacts the desired semiconducting layer. Conversely, the filled NW architecture shown in Figure 3 (c) has the advantage that a continuous, planar contact can be easily applied on top of the semiconductors.

## 2.2 Nanostructured Solar Cell Performance

### 2.2.1 Radial p-n Junction Cells

A variety of the semiconducting nanowire architectures discussed in the preceding section have been employed in inorganic solar cells in an effort to improve charge collection. The performance parameters of some nanostructured p-n junctions are summarized in Table 1. The short-circuit current density ($J_{sc}$) is the current resulting from light absorption when the cell is measured in a short-circuit configuration, such that there is no potential difference across it. The open-circuit voltage ($V_{oc}$) is the voltage formed across the cell in an open-circuit configuration. The power conversion efficiency (PCE) is the most fundamental measure of solar cell performance and is defined as the ratio of the electric power delivered to the external circuit to the solar power incident on the device. Finally, the fill factor FF is the power produced at the maximum power point on the $J - V$ curve divided by the product of $V_{oc}$ and $J_{sc}$. It can be thought of as a measure of how rectangular the $J - V$ characteristic is.

Another measure of photovoltaic performance that is often cited is the external quantum efficiency (EQE). It is the ratio of electrons collected by the solar cell to the number of incident photons at a particular energy (with no correction for reflection losses). It depends on the proportion of light that is reflected, the percentage of non-reflected light that is absorbed, and the efficiency with which photogenerated electron-hole pairs are collected from the cell.

Early attempts at radial Si NW cells employing CVD coatings on VLS and MCEE NWs resulted in poor efficiencies [24, 25, 34]. The $V_{oc}$ values of these cells were quite low, which was attributed to shunt paths through the semiconducting layers, unoptimized diameter distributions of the core-shell structures, and excessive recombination at the large interface and surface areas, as well as at impurities introduced by VLS catalysts. Preliminary work on radial NW cells using GaAs NW arrays showed promising short-circuit currents, but $V_{oc}$ values were similarly low, which

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| Cell Architecture and Synthesis Method | $J_{sc}$ (mA/cm$^2$) | $V_{oc}$ (mV) | FF | PCE (%) |
|---|---|---|---|---|
| PECVD of n-type a-Si:H on disordered VLS p-Si NWs [25] | 1.67 | 130 | 0.28 | 0.1 |
| CVD of i-n polycrystalline Si on individual VLS p-Si NWs [24] | 16.0–23.9 (0.503 pA) | 260 | 0.55 | 2.3–3.4 (72 pW) |
| LPCVD of p-type nanocrystalline Si on disordered n-Si NWs from MCEE [34] | 4.8 | 290 | 0.33 | 0.46 |
| Diffusion doping of periodic 5 μm Si NWs etched from silica bead template on 8 μm n-Si substrate [37] | 16.5 | 525 | 0.56 | 4.8 |
| Diffusion doping of periodic 5 μm Si NWs etched from silica bead template on 20 μm n-Si substrate [37] | 16.8 | 519 | 0.61 | 5.3 |
| Diffusion doping of 2 μm Si MCEE nanohole array in p-Si substrate (patterned by UV lithography) [36] | 32.2 | 567 | 0.52 | 9.5 |
| Radially-doped VLS GaAs NWs from MBE [27] (260 mW/cm$^2$) | 201 μA | 200 | 0.267 | 0.83 |
| CVD of p-CdTe on uniform n-CdS nanopillars grown by VLS in AAO template [38] | 21 | 620 | 0.43 | 5.6 |

**Table 1.** Performance of inorganic cells with nanostructured p-n junctions under standard AM 1.5G illumination (100 mW/cm$^2$ unless specified otherwise).

| Cell Architecture and Synthesis Method | $J_{sc}$ (mA/cm$^2$) | $V_{oc}$ (mV) | FF | PCE (%) |
|---|---|---|---|---|
| $POCl_3$ diffusion doping of MCEE Si NW ARC on monocrystalline Si [29] | 26.1 | 548.5 | 0.65 | 9.3 |
| $POCl_3$ diffusion doping of MCEE Si NW ARC on polycrystalline Si [29] | 21.0 | 475.6 | 0.474 | 4.7 |
| $POCl_3$ diffusion doping of MCEE, slantingly-aligned Si NW ARC on monocrystalline Si [30] | 27.1 | 580.3 | 0.722 | 11.4 |
| VLS of n-Si NW ARC on monocrystalline p-Si wafer [26] | 2.0 | 280 | 0.2 | 0.1 |

**Table 2.** Performance of inorganic photovoltaics with nanostructured anti-reflective coatings under standard AM 1.5G illumination (100 mW/cm$^2$).

was attributed to shunt paths resulting from non-uniform core-shell structures [27].

Garnett et al. increased the PCE of radial Si NW solar cells to over 5 % using Si NWs that were etched from a n-Si wafer using a silica bead template then diffusion doped to form a p-type shell [37]. The template etching method avoided recombination issues associated with VLS NWs, and diffusion doping ensured conformal covering of the NW array with a doped layer, as well as providing intimate contact between the p and n materials. Variable NW length studies in this work showed that the $V_{oc}$ and FF of these cells decreased with increasing nanowire length due to enhanced recombination at the larger interface and surface areas, while the $J_{sc}$ increased, which was attributed to greater light trapping. A significant reduction in reflectance and enhanced absorption have been observed for Si microwire and nanowire arrays by a number of groups, which are attributable to multiple reflections within the sub-wavelength nanostructured architecture [25,29,35,37,51]. Garnett et al. for example, measured a light trapping path length enhancement factor of up to 73 for periodic silicon nanowire arrays [37]. Light-trapping and plasmonic techniques in photovoltaics have been treated in recent reviews [52–54], and will therefore not be discussed in detail here. In a variation of the NW architecture, Peng et al. recently achieved efficiencies above 9 % in radial p-n junction Si cells fabricated by diffusion doping nanohole arrays produced by MCEE [36].

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Promising efficiencies above 5 % were also measured for nanostructured CdS-CdTe heterojunctions [38]. The authors noted that while the PCE of the nanostructured junctions was lower than that of planar junctions with an optimal CdTe thickness, it is higher than the efficiency of planar junctions with comparable CdTe thickness. Notably, the nanostructured cells were produced on aluminum foil substrates and illuminated through top Cu/Au contacts, which only transmitted approximately half of the incident light. Thus significant further gains in the PCE should be possible through optimization of the top contact.

#### 2.2.2 Nanostructured Anti-Reflective Coatings

Better performance has thus far been achieved in Si cells with planar p-n junctions, where the NW structure serves only as an antireflective coating, rather than a nanostructured junction, as in the architecture illustrated in Figure 8 (c). Some results for these cells are summarized in Table 2.

The group of Prof. Jing Zhu have diffusion doped MCEE Si NWs in completion, such that the p-n junction was formed between the base of the nanowires and the substrate [29]. Higher power conversion efficiencies (up to 9.3 %) were observed than for the nanostructured p-n junctions reported in Table 1. They further increased efficiencies beyond 11 % by improving the continuity of the contact electrode using slantingly-aligned NW arrays [30]. These results suggest that increased recombination at the larger p-n interface is responsible, at least in part, for the relatively low efficiencies observed in the nanostructured junction solar cells in Table 1. The PCE of the cells in Table 2, however, is still less than that of standard planar Si cells with anti-reflection coatings, despite the excellent antireflecting properties demonstrated by the NW arrays. This indicates that surface recombination at the dramatically increased interfacial area between the semiconductor and top contact is likely also an issue.

#### 2.2.3 Performance Outlook

The inferior performance of the nanostructured p-n junction and ARC solar cells summarized in Table 1 and Table 2, as compared to conventional planar cells, can be largely attributed to enhanced recombination of photogenerated electron-hole pairs at the ultrahigh interfacial areas created by the nanostructured architecture. Surface recombination occurs in solar cells at the outer surface of the semiconductor, where photogenerated charges can become trapped at defect states arising from broken bonds and extrinsic impurities [4]. Surface recombination is limited in conventional solar cells using passivation and surface field techniques [4]. Most of the nanostructured p-n junctions summarized in Table 1 have an architecture similar to that shown in Figure 3 (b), resulting in a large surface area, as do all of the nanostructured ARCs summarized in Table 2. The high surface to volume ratio is expected to increase the number of surface defects and dangling bonds and hence accelerate the surface recombination of photogenerated minority carriers. Indeed, minority-carrier lifetime measurements have indicated a significantly higher recombination rate in Si NW arrays than in bulk Si [29, 30]. Moreover the minority carrier lifetime was observed to decrease with increasing nanowire length, clearly highlighting this relationship [29]. Thus, appropriate surface passivation techniques are critical for nanostructured devices, but have received little attention at this stage. Cui et al. observed over an order of magnitude increase in the carrier mobility of Si NWs when the surface was passivated, emphasizing the importance of such treatments [55]. Incorporation of processing steps to passivate the large surface areas should therefore improve the efficiency of many of the nanostructured cells listed in Tables 1 and 2. The aforementioned nanostructured CdS-CdTe solar cells on the other hand, which have one of the highest reported PCEs of those listed in Table 1, have a filled nanorod architecture, similar to that shown in Figure 3 (c). As a result, a top surface area, and hence a surface recombination rate, similar to that of a planar junction is expected.

Likewise, a larger p-n junction area is expected to reduce the resistance to recombination current at this interface, also know as *dark current*. This current opposes the photocurrent and a reduction in resistance to its flow typically manifests itself as reduction in the $V_{oc}$ and FF of the solar cell. Indeed, the largest open-circuit voltages and fill factors are observed for the Si cells employing nanostructured ARCs (Table 2), where the p-n junction area is similar to the planar area of the cell. For most of the comparable nanostructured Si p-n junctions in Table 1, the $V_{oc}$ and FF are lower. It is therefore critical that nanostructured solar cells be designed such that the benefits arising from shorter charge transport distances and light-trapping effects outweigh the detrimental effects of increased recombination at the solar cell surface and p-n junction, which should both ideally be limited by careful synthesis of these interfaces. For example, for radial Si NW p-n junctions, it was observed that the increase in $J_{sc}$ with increasing NW length was offset by concurrent decreases in the $V_{oc}$ and FF [37].

Kayes et al. examined the physics of radial p-n junction solar cells and showed that the benefit of better charge collection can outweigh the downside of larger interface and junction areas [56]. Their studies indicated that radial nanowire structures can improve carrier collection and the overall efficiency with respect to planar geometries when the minority carrier transport lengths are small and the recombination rate in the depletion layer is suitably small. Their conclusions have been supported by experimental results. Fan et al. systematically increased the exposed length of the CdS nanopillars in their nanostructured CdS-CdTe junctions from 0 nm (only top of the pillars in con-

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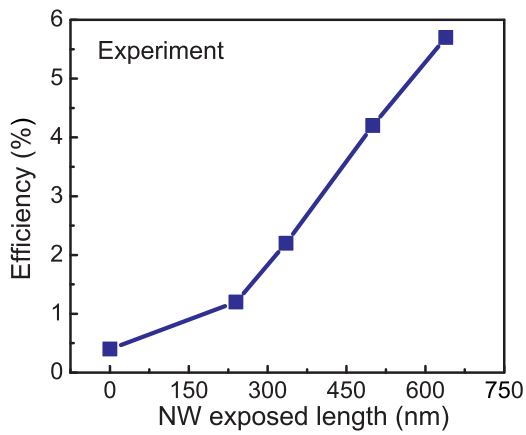


**Figure 9.** Power conversion efficiency of nanopillar CdS-CdTe solar cells as a function of exposed CdS nanopillar length. Nanostructuring of the junction improves carrier collection significantly. (Reprinted by permission from Macmillan Publishers Ltd: Nature Materials [38], copyright 2009.)

tact with the CdTe) to 640 nm and observed more than an order of magnitude increase in power conversion efficiency, as shown in Figure 9 [38]. Hence, the improvement in carrier collection efficiency drastically outweighed any increase in recombination associated with the larger junction area. Thus, significant efficiency gains are possible in nanostructured solar cells employing traditional inorganic semiconductors. Enhanced performance, however, will rely on many factors including careful processing of the nanostructured interfaces, appropriate surface passivation treatments, and the application of continuous low-resistance contact electrodes.

#### 2.2.4 Cost Outlook

While this discussion has focused on the efficiency of various nanostructured inorganic solar cells, we now shift our attention to the cost of these devices. The motivation for this work is to enable the use of lower grade materials and cheaper fabrication methods to improve the performance : cost ratio of solar cells. Many of the nanostructuring methods discussed so far require expensive starting materials and processes, and thus it is important to consider how easily such methods can be applied with cheaper materials and fabrication techniques. For example, the MCEE and templating methods discussed for producing Si NW arrays make use of a starting silicon wafer. This is advantageous in that the resulting nanostructures inherit the good electrical properties of the crystalline substrate, however the cost of crystalline silicon is prohibitively expensive, as discussed in Section 1.2. Further research is therefore needed in applying these nanostructuring techniques to films of polycrystalline Si and other inexpensive semiconductors on low-cost substrates. Preliminary efforts have been made in this direction. Silicon NW arrays have been fabricated from polycrystalline Si films on glass by MCEE [57], VLS Si NWs have been produced on a multicrystalline Si layer on glass [26], and VLS Si NW arrays have been embedded in supporting polymer films [58, 59].

The light trapping capabilities of nanostructured architectures are particularly relevant to cost analysis, as the amount of material required for cell synthesis can be greatly reduced. Kelzenberg et al., for example, recently displayed that absorption similar to that in a commercial planar polycrystalline Si cell can be achieved with a Si microwire array containing only 1 % as much silicon [51]. Appropriate structures could therefore permit significant cost reductions in traditional crystalline solar cells by reducing the required absorber thickness. The synthesis of solar cells with nanostructured ARCs and axial nanowire junctions, however, will still be constrained by the ability of minority carriers to diffuse to the interface along the length of the nanostructure. Minority carrier diffusion lengths of 2 to 10 μm, have been measured in VLS Si NWs [78, 79]. Simultaneous attainment of high absorption, efficient carrier collection, and low materials cost and usage will therefore be challenging. Conversely, in radial p-n junctions with architectures such as that shown in Figure 3, the nanostructure diameter can be tuned to match the diffusion length of minority carriers and the thickness can be freely tailored to maximize light trapping and absorption. Radial nanostructured geometries should therefore more readily enable the design of nanostructured solar cells with smaller amounts of less-crystalline, lower-grade semiconductors.

## 3 Can We Make Truly Low-Cost Solar Cells?

### 3.1 Requirements for Ultra-Low-Cost Inorganic Solar Cells

The device architectures discussed in the previous section may enable the use of smaller amounts of lower-grade, inexpensive semiconductors, however their fabrication methods still involve the use of energy-intensive thermal and vacuum-based techniques. Thus while significant reductions in the cost per watt may be possible, further research and analysis is required to determine whether truly inexpensive, widescale photovoltaic electricity generation is achievable using these materials and synthesis methods. A recent report emphasized the high energy and materials requirements of modern vacuum deposition techniques, and stressed the need for less energy-intensive alternatives such as deposition from solutions [80]. Solution-based deposition routes have the advantage of being low-temperature and scalable, which make them suitable for wide-scale fabrication of inexpensive solar cells on a variety of supporting substrates. In addition to the fabrication of traditional solar panels, the ability of many solution synthesis methods to coat non-planar objects makes them particularly interesting

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| Material | Band gap (eV) | Solution-based synthesis |
|---|---|---|
| $FeS_2$ | 0.8–0.9 [60] | electrodeposition [61], spray pyrolysis [62], electrophoretic deposition of hydrothermally synthesized sol-gels [63] |
| amorphous Si | 1.7 [4] | electrodeposition [64] |
| $Zn_3P_2$ | 1.55 [65] | electrodeposition [65] |
| $Cu_2S$ | 1.2–1.5 [66, 67] | electrodeposition [66], anodic synthesis on Cu substrates [68] |
| CuO | 1.2–1.3 [69, 70] | electrodeposition [70, 71], spray pyrolysis [72], solution-solid reactions on Cu substrates [69] |
| $Cu_2O$ | | electrodeposition [73], photochemical deposition [74] |
| $Cu_2ZnSnS_4$ (CZTS) | 1.45–1.6 [75] | sequential electrodeposition and annealing [75], spray pyrolysis [76], colloidal nanocrystals [77] |

**Table 3.** Abundant and inexpensive inorganic photovoltaic materials.

for the integration of photovoltaics into components with various form factors. The integration of solar cells into construction materials and consumer goods has been limited to niche applications, but low-cost photovoltaic coatings produced from solution have the potential to make significant inroads into these markets.

Another important criteria for low-cost solar cells is materials availability. For example, while it was noted in Section 1.2 that CdTe solar cells can provide a significant cost per watt reduction compared to silicon, it was previously estimated that 0.3 TW of installed capacity would be achievable with existing mineral reserves before tellurium scarcity becomes a limiting factor in cost (assuming a 10 % power conversion efficiency) [81]. Furthermore, a maximum production rate of 5 GW/year was estimated, based on current tellurium refinery output. Similar capacity and growth limits of 0.09 TW and 7 GW/year respectively were estimated for $Cu(In,Ga)Se_2$ cells, due to the limited availability of indium. While these achievable production rates are significantly higher than the rate at which photovoltaic systems are currently being installed, they remain dwarfed by growing energy consumption. Thus while CdTe and $Cu(In,Ga)Se_2$ solar cells may be an important part of a diversified renewable energy solution, their potential impact on a 30 TW demand by 2050 is likely limited. The same authors also highlighted the potential danger of introducing large quantities of these toxic elements into the ecosphere through manufacturing and waste handling [82].

In response to the need for low-cost photovoltaic technologies that can displace a large fraction of traditional, carbon-emitting electricity sources, Wadia et al. presented a study of 23 promising inorganic materials for photovoltaics [83]. Nine inorganic materials were identified as having both the potential for annual electricity production in excess of worldwide demand and material extraction costs less than that of crystalline Si [83]. A selection of these materials are listed in Table 3, along with their respective bandgap energies and some previous reports of solution-based synthesis. In their study, the maximum annual electricity contribution was estimated based on the single-junction, theoretical power conversion efficiency limit of the semiconductor. The area of solar cells that could be manufactured from current annual production of the material was calculated assuming an active layer thickness that absorbs 85 % of the incident energy (for wavelengths between 280 nm and the bandgap of the material). The incident solar spectra was taken as the standard global air mass index AM 1.5G with an intensity of $100\,mW\,cm^{-2}$, and a capacity factor of 20 % was assumed. The material extraction costs were calculated from reported mining costs. It is important to note that materials processing and balance of system costs, which can constitute a significant portion of the overall cost, were omitted from this analysis. Two of the nine materials identified, PbS and NiS, have prohibitively low theoretical efficiencies (band gaps of approximately 0.4 eV [84, 85]). Balance of systems costs for photovoltaic systems using these materials would be excessively high on a per watt basis, such that these materials have been neglected in Table 3, despite their significant abundance.

Following from this discussion, several basic requirements for *ultra-low-cost* photovoltaic coatings can be identified:

- Abundant, inexpensive materials
- Low-temperature, atmospheric fabrication of crystalline materials
- Scalable synthesis on low-cost substrates
- Suitable efficiency and stability
- Low-toxicity

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Simultaneous attainment of these criteria is extremely challenging. Zinc phosphide, for example, is a common rodenticide that is very harmful to humans. Amorphous silicon (a-Si) is typically deposited by plasma-enhanced chemical vapour deposition in dedicated vacuum systems [86] and attempts to synthesize it by electrochemical deposition (electrodeposition) from atmospheric solutions have been problematic due to oxidation of the silicon in atmospheric conditions [64]. While such toxicity and stability issues could be addressed with appropriate packaging in some applications, the use of stable, environmentally-benign materials is preferable for the wide-scale deployment of photovoltaic coatings in a variety of applications.

For many of the solution-based synthesis methods listed in Table 3, good-quality, crystalline materials can be achieved but an energy-intensive heating step is required. For example, stoichiometric $FeS_2$ was only obtained when electrodeposition or spray pyrolysis was followed by a 500 °C anneal in a sulfur atmosphere [61, 62], and hydrothermal synthesis of $FeS_2$ required heating at 200 °C for prolonged periods (i.e. 40 hr) [63]. Similarly, CZTS films produced by electrodeposition require annealing of the component layers in a sulphur atmosphere at 550 °C to form the composite structure [75] and the synthesis of CZTS nanocrystals necessitates heating at 280 °C for an hour in an inert atmosphere [77]. In fact, all of the spray pyrolysis methods listed in Table 3 require heating of the substrate during deposition to a temperature of several hundred degrees Celsius [62, 72, 76]. In addition to the energy requirement, the need to heat the material limits the type and size of substrates that can be coated. In particular, inexpensive, flexible plastic substrates cannot be employed when heating to several hundred degrees is involved.

It has been possible to synthesize polycrystalline thin films of some of the stable, non-toxic materials listed in Table 3 from solutions at low-temperature. Polycrystalline $Cu_2O$, $Cu_2S$, and CuO, for example, have been produced by electrochemical deposition near room temperature [66, 70, 71, 73], and polycrystalline CuO has also been produced by a solution-solid reaction on Cu, although excessively long reaction times (i.e. 100 hr) were required [69]. The ability to synthesize abundant photovoltaic semiconductors using low-temperature, solution-based methods will be essential for the widescale implementation of low-cost photovoltaic electricity generation and is an integral area for future research.

Moreover, solution-based synthesis generally results in materials of poorer crystallinity and phase purity than those produced by vacuum deposition methods in ultra-clean environments at high temperatures. Polycrystalline $Zn_3P_2$ films prepared by electrodeposition, for example, contain a large concentration of Cl impurities [65] and $Cu_2S$ formed by anodic synthesis on copper substrates displays a variable stoichiometry through the deposited layer [87]. Greater concentrations of grain boundaries, charge traps, and recombination centres are thus expected, which limit the distances over which photogenerated charge carriers can be transported and collected, reducing $L_C$ in Figure 2 [4]. Thus, techniques need to be developed for producing suitable nanostructures of these solution-synthesized materials that will enable the efficient collection of photogenerated charges.

### 3.2 Low-Cost, Solution-Based Methods For Fabricating Inorganic Nanostructures

Many of the nanostructuring techniques discussed in Section 2.1 can be applied to abundant, low-cost semiconductors such as those listed in Table 3. For example, MCEE techniques similar to those summarized in Section 2.1.2 for silicon could be developed for thin films of relevant semiconductors synthesized from solutions on low-cost substrates. Templating methods have been used to synthesize relevant nanostructured semiconductors from solutions and will be reviewed in this section. Additionally, novel techniques for solution-based self-assembly of nanostructured semiconductors have been demonstrated in recent years and will also be discussed here.

Some of the materials listed in Table 3 cannot be readily synthesized in both n and p-type forms, such that use of complementary semiconductors is necessary. Wide-bandgap semiconductors such as ZnO, $TiO_2$, and $SnO_2$ for example, have been used extensively in heterojunction solar cells, as will be discussed in the following sections. They are transparent to visible light and can therefore be employed as window layers that localize the light absorption near the p-n junction, reducing surface recombination effects. They consist of abundant materials and can be synthesized from solutions, making them well-suited for ultra-low-cost photovoltaics.

#### 3.2.1 Template-Assisted Synthesis of Ultra-Low-Cost Photovoltaic Nanostructures

Electrochemical techniques have been used to deposit a variety of inexpensive semiconductors in mesoporous templates. Many groups have filled anodic aluminum oxide (AAO) templates by electrochemical deposition, then etched away the template to leave free-standing nanorod, nanowire, or nanotube arrays, as was illustrated in Figure 7 (c). In electrochemical deposition, a potential is applied to a conducting substrate in an electrolyte of dissolved precursors, producing an electrochemical reaction which causes the precipitation of the desired material. It is a low-temperature, scalable, inexpensive synthesis technique, which allows considerable control over film thickness and properties via the deposition conditions. It ensures a conductive path between the substrate and the deposited material, and many relevant semiconductors and metals can be deposited in this manner [88–91].

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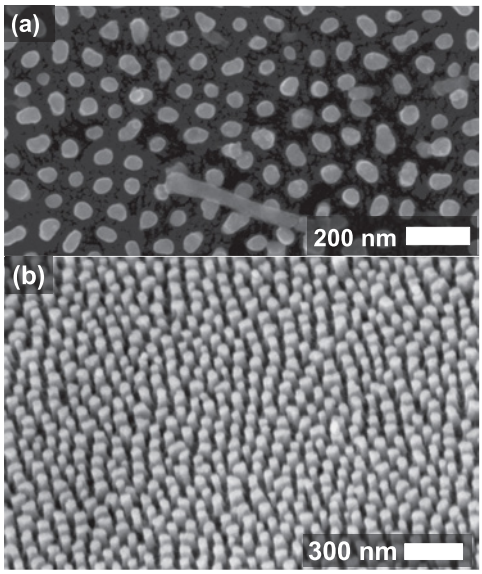


**Figure 10.** Planar (a) and inclined (b) views of freestanding $Cu_2O$ nanorod arrays on conducting glass substrates that were synthesized by electrodeposition into AAO templates [43]. (Copyright Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission.)

Most initial work on producing nanostructured semiconductors (e.g. ZnO, $TiO_2$, $Cu_2O$) using AAO templates utilized thin, unsupported templates poorly suited for device fabrication [47, 90, 92–95]. A metal film was typically deposited on one side of the template to act as the conducting electrode at the base of the nano-sized pores. More recently, various groups have demonstrated the ability to electrodeposit semiconducting nanostructures in AAO templates on supporting substrates, initially crystalline silicon [49, 96–98]. In our laboratory, we have since demonstrated a technique for producing large-area, freestanding nanorod arrays using AAO templates on conducting glass substrates and transparent flexible substrates well-suited for photovoltaic applications [43]. Figures 10 (a) and (b) display an array of freestanding $Cu_2O$ nanorods produced on conducting glass by this method. The ability to finely-tune the spacing and diameter of the nanorods via the anodization and etching conditions will be particularly useful for studying the influence of nanostructure morphology on solar cell performance.

Nanotube and nanorod arrays have also been produced in AAO templates on conducting glass using other techniques such as capillary filling [100] and electrophoretic deposition of sol-gels [101]. In sol-gel techniques, a solid precursor species suspended in a liquid (sol) condenses to form a gel after infiltration into the pores. A thermal treatment, however, is required to transform the gel into the desired material. In electrophoretic deposition, a potential is applied to the conducting substrate to aid in the filling of the pores by the charged sol species.

The synthesis of freestanding nanorod and nanotube arrays using AAO templates does require thin, high-purity Al films to be sputtered onto the supporting substrate in a vacuum. If vacuum-based methods are to be avoided, thin Al foils could instead be used as the supporting substrate, as was done by Fan et al. in their work on nanostructured CdS-CdTe cells, although this does restrict the solar cell to top-side illumination geometries. Alternatively, Byun et al. recently demonstrated a novel technique utilizing a graft polymer to attach an unsupported AAO membrane onto a variety of conducting substrates [102]. This method does not require vacuum-based deposition of aluminum and has the additional advantage that highly-ordered AAO templates fabricated by a two-step anodization method [42] can be employed.

Other nanostructured templates mentioned in Section 2.1, such as self-assembling monolayers and block copolymers, can be readily synthesized from solutions. Relevant nanostructures have been deposited in colloidal tem-

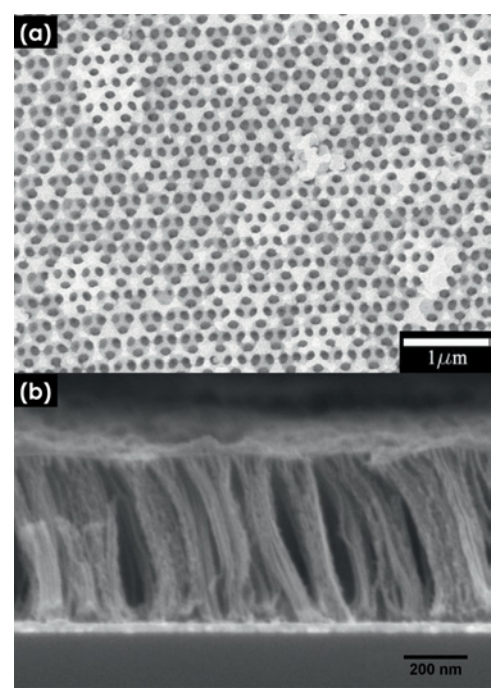


**Figure 11.** (a) Planar view of ordered mesoporous ZnO nanostructure synthesized by electrochemical deposition into a template of polystyrene spheres on conducting glass, followed by removal of the spheres. (Reprinted from [39], Copyright 2005, with permission from Elsevier.) (b) Cross-section of $TiO_2$ nanowire array produced by electrodeposition into a block copolymer template. Bunching of some nanowires is observed due their high aspect ratio. (Reprinted with permission from [99]. Copyright 2009 American Chemical Society.)

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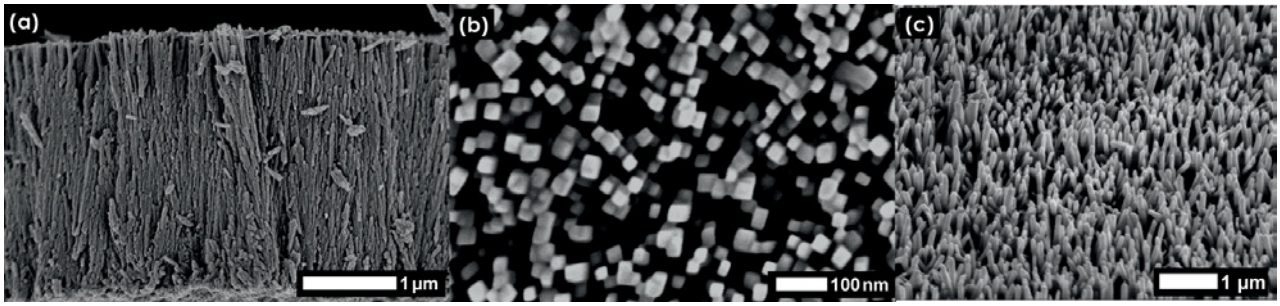


**Figure 12.** (a) Cross-section and (b) planar view of hydrothermally-grown $TiO_2$ nanowire arrays on conducting glass. (Reprinted with permission from [103]. Copyright 2008 American Chemical Society.) (c) Inclined view of electrodeposited ZnO nanowire arrays.

plates consisting of self-assembling layers of polystyrene or silica spheres using methods such as electrodeposition, sol-gel synthesis, and metal salt precipitation from solution [39, 104, 105]. Figure 11 (a) shows an ordered ZnO nanostructure fabricated on conducting glass by electrodeposition into a template of self-assembled polystyrene spheres. The spheres were synthesized by a polymerization technique and applied to the conducting glass surface in solution.

Figure 11 (b) displays a $TiO_2$ nanowire array synthesized by electrodeposition into a block copolymer template [99]. Block copolymers are chemically-distinct polymers covalently bonded at one end that self-assemble into well-ordered structures, including arrays of cylinders. Highly-oriented, nearly defect-free arrays of nanoscopic, cylindrical domains that span film thicknesses up to several microns and have a high degree of long-range lateral order have been produced [44,45]. The cylindrical phase can then be removed, leaving a template to be filled with nanowire material [99, 106, 107]. They can be produced on a variety of supporting substrates by simple spin-coating techniques combined with annealing at moderate temperatures (e.g. 100 to 200 °C), often with an applied electric field to influence polymer alignment. While the control of pore size and spacing in block copolymers is currently less than that achievable for AAO templates, their scalable, solution-based synthesis makes them extremely attractive.

### 3.2.2 Self-Assembly of Ultra-Low-Cost Photovoltaics Nanostructures

In recent years, considerable effort has been dedicated to producing nanostructured semiconductors by self-assembly from solutions. No lithographic patterning or templating techniques are required with these methods and large-area synthesis is possible. Highly-crystalline arrays of ZnO nanowires [46, 108, 109], $TiO_2$ nanowires [103], and $TiO_2$ nanotubes [110] have been hydrothermally grown from aqueous solutions. In hydrothermal growth, anisotropic chemical precipitation occurs in a solution heated to moderate temperatures, resulting in the formation of high aspect ratio nanostructures. Dense and homogeneous arrays can be produced over large areas on various supporting substrates and the dimensions of the wires or tubes can be controlled to some extent via the solution concentration and growth parameters. Figures 12 (a) and (b) display cross-sectional and planar images of $TiO_2$ nanowires grown hydrothermally on conducting glass in a toluene solution at 180 °C.

Arrays of self-assembling crystalline ZnO nanowires have also been electrochemically deposited directly from solution onto a variety of conducting substrates without the use of a template [111, 112]. Again, anisotropic precipitation can result in dense arrays of nanowires with inclination approximately normal to the substrate. Figure 12 (c) displays a ZnO nanowire array synthesized in our laboratory on conducting glass using a typical aqueous zinc chloride solution heated to approximately 75 °C. As with hydrothermal growth, nanowire arrays with a variety of dimensions can be grown by controlling the electrodeposition parameters [113–115]. Nanowires many microns long with diameters on the order of ten nanometers have been achieved. Less control over the spacing and inclination of the nanowires is typically possible, however, than with comparable templating methods.

Highly-ordered arrays of $TiO_2$ nanotubes have also been produced by anodising titanium [116–118]. Paulose et al. for example, produced 3600 nm long, optically transparent $TiO_2$ tubes with 46 nm pore diameters and 17 nm wall thicknesses on transparent conducting substrates [116]. This synthesis technique does, however, require a post-deposition annealing step above 400 °C to produce anatase $TiO_2$.

Coating techniques have also been developed to cover self-assembling nanostructures with relevant semiconducting materials. Foong et al. presented a method where repeated chemisorption/hydrolysis reactions were used to coat substrate-supported AAO templates with thin layers of $TiO_2$ [124]. They referred to this process as *liquid-ALD*, as the observed deposition rates and resulting films were similar to those achieved by conventional gas-phase atomic layer deposition. Qiu et al. produced $TiO_2$ nan-

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| Cell Architecture and Synthesis Method | $J_{sc}$ (mA/cm$^2$) | $V_{oc}$ (mV) | FF | PCE (%) |
|---|---|---|---|---|
| Drop-cast $Cu_2O$ nanoparticles in hydrothermal ZnO NWs coated with $TiO_2$ by ALD [129] | 1.43 | 150 | 0.25 | 0.05 |
| $Cu_2O$ in ZnO NWs (both electrodeposited) [120] | 4.4 | 280 | 0.39 | 0.47 |
| Hydrothermal ZnO NWs filled with PbSe quantum dots from colloidal solution [121] | 18.6 | 420 | 0.25 | 2.0 |
| Electrodeposited 30–40 nm PbSe ETA layer at ZnO NW-CuSCN junction (36 mW/cm$^2$ halogen lamp) [122] | 4.0 | 500 | 0.4 | 2.3 |
| Spray-coated 25 nm $In_2S_3$ ETA layer at hydrothermal ZnO NW-CuSCN junction [123] | 10.5 | 570 | 0.56 | 3.4 |

**Table 4.** Performance of solution-synthesized inorganic cells with self-assembling nanostructures under standard AM 1.5G illumination (100 mW/cm$^2$ unless specified otherwise).

otubes by coating hyrdothermally-grown ZnO NWs using a dip-coating sol-gel method, then selectively etching the ZnO to leave the tubes [125]. In a similar manner, Lee et al. employed a liquid phase deposition method to coat hydrothermally-grown ZnO nanowires with $TiO_2$. Their liquid phase deposition technique relied on the chemical equilibrium between a metal-fluoro complex and metal oxide, and permitted the synthesis of thin, homogeneous coatings. Concurrent dissolution of the ZnO occurred during the liquid phase deposition, such that both $TiO_2$ rods and tubes were formed [126]. These $TiO_2$ coatings, however, do require annealing at several hundred degrees for crystallization. Conversely, a hydrothermal method presented for coating self-assembling ZnO nanowires with thin MgO coatings was performed entirely below 100 °C [127]. Such solution-based coating techniques will enable the incorporation of a wider variety of semiconductors in low-cost nanostructured solar cells. Self-assembling structures, such as the nanowire and nanotube arrays presented in this section, could be used as nano-scaffolding for coated solar cell architectures like that shown in Figure 3 (a).

### 3.3 Performance of Ultra-Low-Cost Nanostructured Inorganic Solar Cells

Low-cost nanostructured inorganic solar cells synthesized from solutions have received considerably less attention than their counterparts fabricated from more traditional photovoltaic materials by vacuum-based methods. However, self-assembling nanostructures, particularly ZnO and $TiO_2$ nanowire and nanotube arrays, have been employed extensively in dye-sensitized and hybrid organic-inorganic solar cells, and are now being introduced into more stable, low-cost inorganic cells. Most architectures have involved filling the transparent NW array with an appropriate absorber, as illustrated in Figure 3 (c). The performance of several ultra-low-cost nanostructured inorganic solar cells is summarized in Table 4.

Yuhas et al. drop-cast $Cu_2O$ nanoparticles (a p-type semiconductor) into a hydrothermally-grown ZnO NW array. Photovoltaic behaviour was not observed however, until the wires were coated with 10 nm of $TiO_2$ by vacuum-based atomic-layer deposition. The coating was believed to prevent shorting through the ZnO NW array, although the resultant PCE remained quite small at 0.05 % [129]. Additionally, annealing at several hundred degrees was required to obtain suitable contact between the $Cu_2O$ nanoparticles, which would prevent the fabrication of such cells on flexible plastic substrates. In recent work, we improved the ZnO NW-$Cu_2O$ heterojunction design, resulting in an order of magnitude increase in the PCE [120]. $Cu_2O$ was electrodeposited into arrays of freestanding ZnO NWs, which were also grown by electrodeposition on conducting glass substrates. This produced a $Cu_2O$ absorbing layer of higher crystallinity and a continuous ZnO-$Cu_2O$ interface for charge separation, as seen in Figure 13 (a). The EQE was observed to increase with ZnO NW length, as shown in Figure 14, reaching values of 85 % without any antireflection coatings. The increase in EQE with NW length was attributed to both minority carrier collection from further within the Cu2O layer and enhanced photon absorption near the Cu2O-ZnO interface, arising from light scattering by the ZnO NWs. A $J_{sc}$ value of 5.4 mA/cm$^2$ was measured in cells with a 2 μm $Cu_2O$ absorbing layer and approximately 1 μm long NWs, higher than previously reported for equivalent planar cells with thicker absorbing layers [129]. Concurrent work employing longer NWs reported $J_{sc}$ values above 8 mA/cm$^2$ under non-standard illumination [128]. The nanostructured $Cu_2O$-ZnO devices we

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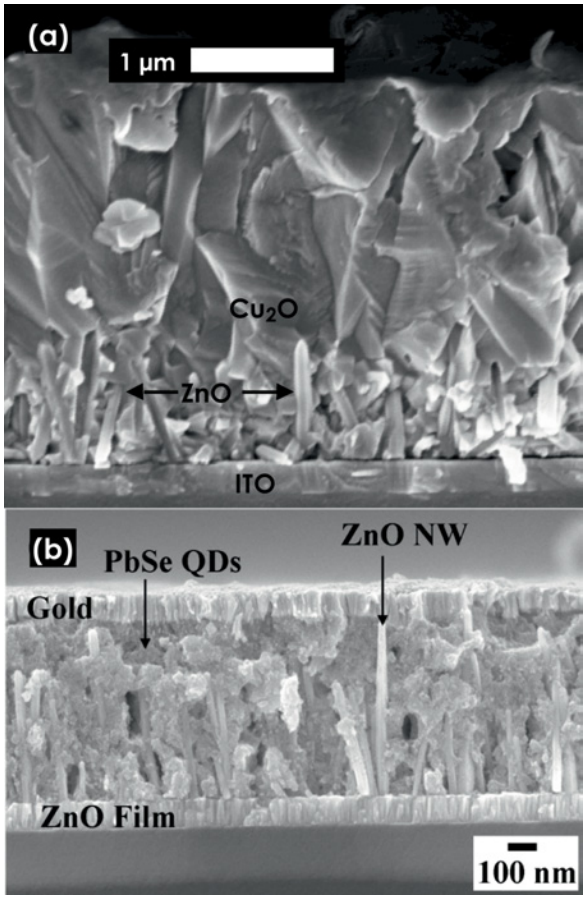


**Figure 13.** (a) Cross-section of a nanostructured $Cu_2O$-ZnO solar cell electrochemically deposited from solutions near room temperature [120]. (Copyright Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission.) (b) Cross-section of a nanostructured ZnO-PbSe solar cell synthesized by dip-coating hydrothermally-grown ZnO NWs with PbSe quantum dots. (Reprinted with permission from [121]. Copyright 2009, American Institute of Physics.)

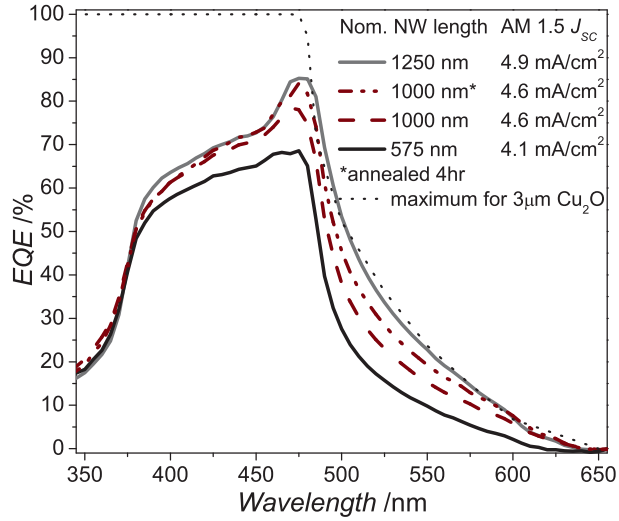


**Figure 14.** External quantum efficiency of $Cu_2O$-ZnO NW solar cells with a 3 µm $Cu_2O$ absorbing layer and various nominal nanowire lengths. Clear enhancements in carrier collection and $J_{sc}$ were observed with increasing nanowire length. The absorption was observed to surpass that expected for a 3 µm $Cu_2O$ layer, indicating enhanced absorption due to light-scattering by the NWs [120]. (Copyright Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission.)

have developed can be fabricated on short time scales from solutions near room temperature, making them well-suited for a variety of inexpensive substrates [120]. Their reported efficiencies, however, are still less than that of planar equivalents [129] such that optimization of the nanostructure geometry and materials properties is required. In recent work, it was demonstrated that care must be taken when processing ZnO nanostructures in aqueous solutions, and a novel buffering method was developed to improve the properties of the electrochemically synthesized $Cu_2O$-ZnO interface [130].

Leschkies et al. obtained a higher efficiency of 2 % by filling hydrothermal ZnO NW arrays with PbSe quantum dots [121]. The PbSe was applied by dip coating the NWs in colloidal solutions, resulting in the device structure shown in Figure 13 (b). As for the $Cu_2O$-ZnO NW cells, the $J_{sc}$ and PCE were observed to increase with nanowire length for a fixed PbSe layer thickness, indicating improved charge collection.

Of the various nanostructured inorganic solar cells that could be qualified as *ultra-low-cost*, extremely thin absorber (ETA) cells have received the most attention. The ETA design is based on a semiconducting, extremely thin absorbing layer sandwiched between transparent, highly-interpenetrated electron and hole-transporting semiconductors. It is similar to the architecture shown in Figure 3 (c), but with both the n and p layers transparent to visible light and a thin absorbing layer (thickness on the order of 10 nm) located at the interface. The large interfacial area of the nanostructured junction facilitates the use of a thin absorbing layer that can efficiently transport photogenerated carriers to the adjacent electron and hole conductors, while providing suitable absorption. As with the other nanostructured geometries, direct pathways for charge transport and possible light trapping enhancements are also provided. Levy-Clement et al. were the first to report an ETA cell of notable performance [122]. It consisted of a self-assembling ZnO NW array on conducting glass that was sensitized with a 30 to 40 nm layer of CdSe (both the ZnO and CdSe were electrodeposited) and filled with transparent copper(I) thiocyanate (CuSCN) from solution. A PCE of 2.3 % was measured under non-standard illumination, although the elec-

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trodeposited ZnO-CdSe core-shell structures required annealing at 350 °C. A power conversion efficiency of 3.4 % has since been achieved in ETA cells employing a spray-coated $In_2S_3$ absorber on hydrothermal ZnO NWs, again with with CuSCN as the hole conductor [123,131]. A lower annealing temperature of 200° was applied to these devices. Although more expensive semiconductors have been employed as the absorbing layers in ETA cells, the small quantity of material required may keep the cost suitably low. Levy-Clement et al. noted, for example, that the absorption of the 40 nm CdSe layer in their ETA cell was similar to that of a 100 μm layer of crystalline Si [122].

Thus while nanostructured inorganic solar cells fabricated by low-temperature, solution-based methods have received less attention than dye-sensitized and hybrid organic-inorganic devices, their inherent greater stability makes them of considerable interest, and significant progress in their development has been made in the past few years. There is much room for further improvement through dimensional control of self-assembling nanostructures, study of interfacial properties of p-n heterojunctions synthesized from solutions, the introduction of low-cost electrode materials, and implementation of such devices on low-cost substrates.

## 4 Conclusions

In this review, the motivation, methods, challenges, and prospects for nanostructured inorganic solar cells were discussed. For nanostructured solar cells consisting of traditional photovoltaic semiconductors, efficiencies have improved considerably in recent years and will undoubtedly approach those of equivalent planar cells with further research and development. P-n junction design, surface passivation, and application of contact electrodes, among other processes, will need to be improved to make these efficiency gains. Through careful selection of the materials and processes employed, as well as the cell geometry, significant cost reductions should be possible by reducing the quantity and quality of the materials used. Detailed economic analysis is warranted to determine what cost reductions may be achieved for nanostructured cells employing traditional semiconductors.

The development of ultra-low-cost inorganic solar cells, which utilize abundant materials and inexpensive solution-based fabrication methods, deserves similar attention. Although very much in their infancy, these devices are inherently more stable than organic-based equivalents and are extremely promising as cheap solar cells. The use of appropriate nanostructures is particularly important to achieve suitable charge collection in these cells and further research is required in producing such nanostructures and implementing them in devices. Further economic analysis is also necessary to determine what power conversion efficiencies need to be achieved to ensure that reductions in the cost of cell fabrication translate into actual reductions in the cost per watt of electricity produced. Through continued development of nanoscale materials and devices, inexpensive solar power can become a reality.

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