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P. Riederer, M. Bouraoui, and R. Kersting[a)]

AFFILIATIONS

Photonics and Optoelectronics Group, Faculty of Physics and Center for NanoScience (CeNS), Ludwig–Maximilians-Universität, Königinstr. 10, 80539 München, Germany

[a)]Author to whom correspondence should be addressed: roland.kersting@lmu.de

ABSTRACT

The interface roughness between gate insulator and semiconductor is expected to reduce the conductance of molecular field-effect transistors. This study merges atomic force microscopy data of layer topographies with self-consistent calculations of charge carrier densities and conductances within the channel region. It is found that a roughness equivalent to one monolayer reduces the conductance by nearly 50%. Currents flow mainly within the first monolayer of the semiconductor and along percolation pathways, where charges rarely undergo transfers between adjacent monolayers.

Record charge carrier mobilities in molecular semiconductors are reported nearly every year and are currently approaching values where technical applications are coming within reach.[1–4] However, until now the mobilities in molecular field-effect transistors (FETs) have been much smaller than those in silicon devices, and the reasons are under debate. Discussed, for instance, are the small widths of the electronic bands of organic semiconductors,[5,6] polaronic effects,[7,8] dynamic localization of the charge carriers,[9,10] and the roughness of the gate insulator.[11]

Recent experimental work on molecular FETs has shown that an increased surface roughness of the gate insulator leads to a larger density of grain boundaries, which reduces the effective carrier mobility.[12] We report how roughness on its own diminishes the channel conductance. We will show that a root mean square (RMS) roughness equivalent to one monolayer reduces the conductance by about 50%. Currents mainly flow along percolation pathways within the first monolayer. Thermally activated transfers between monolayers rarely occur.

In the first step of this work, we investigate how surface roughness affects the distribution of free carriers within the molecular semiconductor at the interface to the gate insulator. In the second step, we conclude from the charge distribution on the conductance of the channel. Such a study would be challenging using exclusively experimental means, because the accumulation region is cladded between the gate insulator and semiconductor layers above, and thus, is not directly accessible. Therefore, we combine experimental data of the layers' surface topographies with self-consistent calculations of the interplay between roughnesses, local potentials, and charge carrier distributions within the channel.

The layer topographies are recorded on devices as described in Ref. 13. Figure 1 displays the layer sequence. The gate contact is an 6 nm thick chromium layer, and the injection layer consists of 3 nm MoO_x topped by 6 nm chromium. Both contacts, as well as the molecular semiconductor 2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C8-BTBT-C8), are fabricated by physical vapor deposition. The gate insulator is obtained by chemical vapor deposition of parylene N.[14] The thicknesses of the insulator and of the C_8-BTBT-C_8 are $t_{ins} \approx 300$ and $t_{sem} \approx 40$ nm, respectively. The topographies of the individual layers are obtained by atomic force microscopy (AFM). Typical RMS values are shown in Fig. 1. The most important value for this work is the roughness of the gate insulator Δz_{ins}.

The charge carrier distributions are calculated for volumes as illustrated in Fig. 1. We assume that a gate voltage is applied between bottom and top contact, which leads to the injection of holes from the top-contact and their accumulation at the interface between the C_8-BTBT-C_8 semiconductor and the parylene N gate insulator. Two main effects define the distribution of free holes along this interface: (i) The applied voltage and the roughness of the interface cause potential wells where holes accumulate. Local hole densities can approach 10^{19} cm^{-3} as we show later. (ii) At such densities, strong Coulomb forces between the injected holes arise. They screen the electrostatic potentials, which in turn modifies the charge carrier distributions.

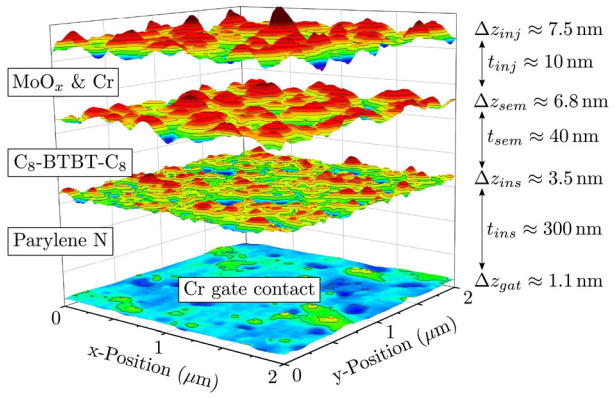

FIG. 1. Illustration of the layer topographies of the investigated structure. The thicknesses t_i of the layers are not to scale, but the roughnesses Δz_i are. All micrographs are recorded at different spots.

The overall potential landscape within the device is obtained by the self-consistent solution of the Poisson equation by considering the carrier statistics that regulate the local charge density.[15] Usually, Maxwell–Boltzmann statistics are applied. In this work, however, the Fermi energies approach the valence band and Fermi–Dirac statistics are appropriate. Volumes as illustrated in Fig. 1 are discretized by $100 \times 100 \times 100$ nodes. The node spacing perpendicular to the layers is set to 4 nm, which is close to typical values for the long axes of unit cells found in molecular semiconductors with substituents, such as aromatic rings and long alkyl groups.[16,17] Within the layer plane, the nodes are 20 nm apart, which corresponds to the lateral resolution of the AFM data. Discretizing the Poisson problem leads to a sparse system of equations that can be solved by iterative methods. The computational costs are efficiently reduced by applying listing concepts.[15,18] All data presented are obtained using a damped Newton–Raphson algorithm combined with the method of successive overrelaxation.

Throughout this work, an external bias between the gate and the injection layer of $V_{ext} = 50$ V is assumed, which leads to a sheet density of $n_{2D} \approx 2 \times 10^{12}$ cm^{-2} of accumulated holes. For all calculations, the effective mass of the holes is set to the free electron mass.[19,20] Between the molecular semiconductor and the MoO_x injection layer, a Schottky barrier of 0.2 eV is assumed. The relative permittivities of the insulator and the molecular semiconductor are set to 2.7 and 2.8, respectively.[21–23] However, these values change with the choice of materials; the selections made above are intended to overlap with previous studies on similar materials.

Figure 2 shows lateral cross sections through the simulated device within the interface region between the semiconductor and the insulator. Displayed are the material distribution (a), local potentials (b), and hole densities (c) and (d). In this particular calculation, the RMS roughness of the gate insulator is $\Delta z_{ins} = 3.5$ nm, and the lattice temperature is set to $T = 300$ K. The composition map in Fig. 2(a) illustrates the material inhomogeneity at the interface between the gate dielectric and the semiconductor. Figure 2(b) shows the local potential ϕ, which is the superposition of the externally applied bias V_{ext} and the Coulomb potential due to accumulated holes around a specific node. The local valence band edge is $E_{vb,loc} = E_{vb,mat} - e\phi$, where $E_{vb,mat}$ is the material's valence band edge. Thus, negative potentials

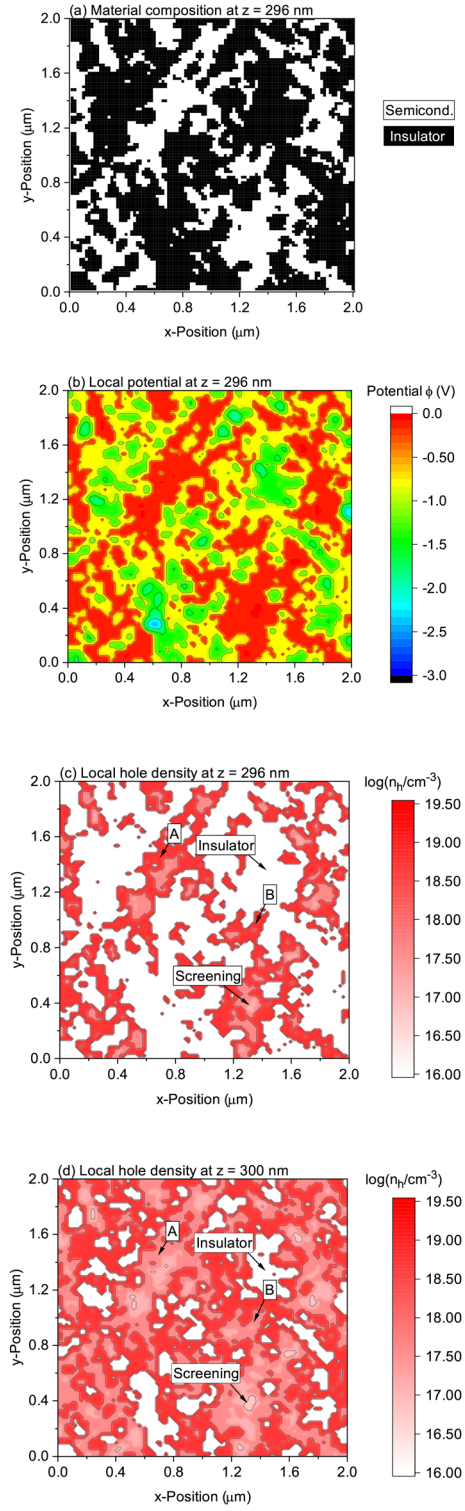

FIG. 2. Cross sections through the simulated volume at $z = 296$ nm from the gate contact (a)–(c) and at $z = 300$ nm (d). (a) Material composition. (b) Local potential ϕ. (c) and (d) Local hole densities.

draw the valence band edge toward the Fermi energy, which leads to the accumulation of holes.

Local densities of accumulated holes n_h are shown in Fig. 2(c). Areas without any carriers mirror the insulator regions. All other areas can be attributed to potential wells of the semiconductor, as shown in Fig. 2(b). Within the wells, the charge carrier densities vary between 10^{16} and $10^{19}\,\mathrm{cm}^{-3}$. These regions show one peculiarity caused by the Coulomb interaction between the injected holes. In nearly all of the red shaded regions, the hole density n_h is smaller near the center of the region than at its border. The high density of the holes screens the wells' potentials and draws the local band edges from the Fermi energy, which in turn reduces the charge densities within the wells. Further calculations not displayed here show that lateral screening reduces charge carrier densities within the puddles to about 50%.

One monolayer further apart from the interface, the holes cover nearly the entire cross section, as shown in Fig. 2(d). Only a few insulating islands remain. The hole densities displayed in Figs. 2(c) and 2(d) also illustrate the efficiency of Coulomb screening perpendicular to the layers. This becomes visible when comparing spots, such as those indicated by A and B. These regions have high charge carrier densities within the lower layer and drastically reduced densities one layer above.

Details of how the screened potential ϕ affects valence band edges $E_{vb,loc}$ and hole densities n_h are provided in Fig. 3. In equilibrium, the Fermi energy is constant across the device. The gradient of the band edge within the insulator mirrors the externally applied field. In contrast, the valence band within the semiconductor is nearly flat and close to the Fermi energy. At the maxima of the valence band, the hole densities approach $10^{19}\,\mathrm{cm}^{-3}$, as shown in Fig. 3(b). Such densities cause efficient field screening in the direction toward the injection layer. The carrier densities drop by orders of magnitude with increasing z, similar to those discussed for homogeneous layers.[24] One consequence is that the roughness of the interface with the insulator has a much bigger impact on transport properties than the roughness of the interface of the injection material. Therefore, in the following, we exclusively focus on the impact of the insulator roughness Δz_{ins} on charge transport.

According to the data of Fig. 3(b), about 95% of the charge carriers are accumulated within the first two monolayers, which corresponds to a layer thickness of about 8 nm. In this region, the local potential ϕ shifts the valence band edge $E_{vb,loc}$, as illustrated in Fig. 4 along the plane of the interface. From one monolayer to the next, the potential changes by about 70 mV, equivalent to a shift of the band edge by nearly $3\,k_BT$, when assuming room temperature. Thus, substantial thermal activation is needed for charge carrier transfers from lower to upper monolayers, whenever such a transfer is required for maintaining current flow between the potential wells. Previous work suggested that the charge transfer is limited by potential barriers between the wells.[11] This framework, however, applies to one-dimensional conductors rather than to two-dimensional surfaces where alternate percolation pathways may sustain conduction. Distinct percolation thresholds have been observed, for instance, in blends of molecular semiconductors and polymers.[25]

In order to determine the conductance along the channel, we assume that the local conductivity σ depends exclusively on the local density n_h at the particular node and the generic mobility μ. For this local mobility, a value of $10\,\mathrm{cm}^2/\mathrm{Vs}$ is assumed, which is close to values

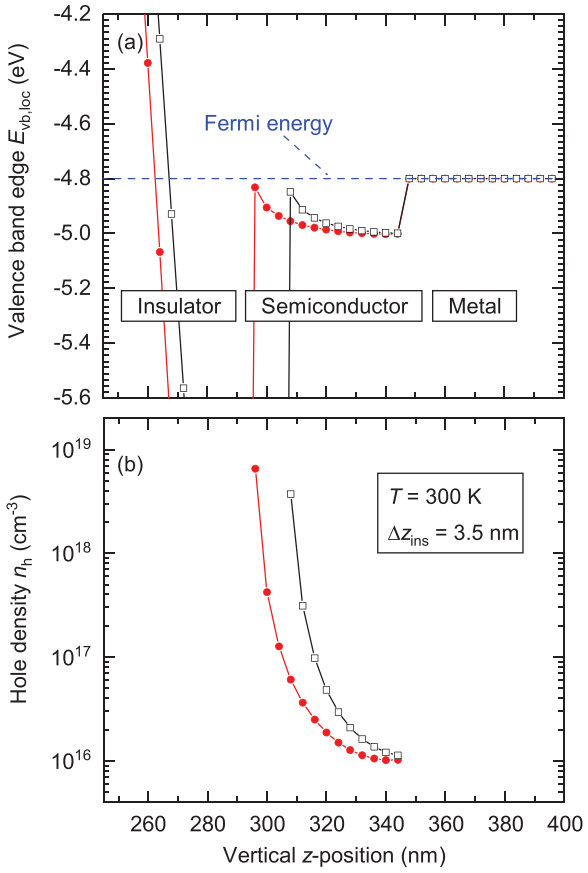

FIG. 3. Results for two distinct xy-positions, which are shown by the red dots and the open black boxes, respectively. (a) Valence band edges of the insulator and the semiconductor. For the metal, the Fermi energy is shown. (b) Hole density in dependence on the distance from the gate contact.

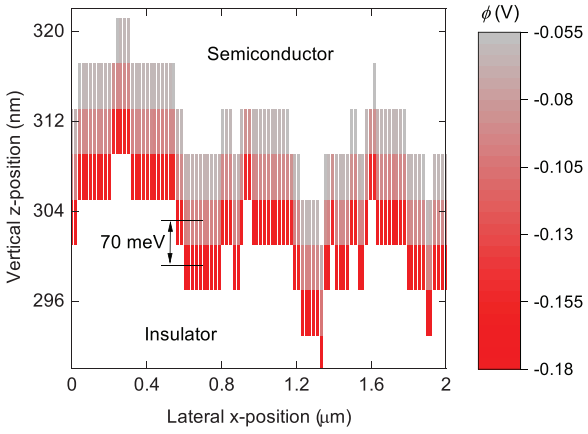

FIG. 4. Heat map of the local potential ϕ for the first three semiconductor monolayers within the xz-plane. The heights and widths of the bars indicate the dimensions of the unit cells between the nodes.

measured, for instance, by terahertz spectroscopy.[13,20] The conductance between two nodes results from their local conductivities. Also included is thermal excitation according to a Maxwell–Boltzmann distribution if the potential difference $\Delta\phi$ between the nodes requires this. Additionally, one may regard that many molecular semiconductors have reduced transfer integrals along the long axis of their unit cells, that is, for transfers between adjacent monolayers. This reduction in the transfer integrals is attributed by introducing the factor f_z that formally reduces the conductance between monolayers. Altogether, this approach describes a network of resistances, and solving the corresponding system of equations provides the sheet conductance $G_\square$. The impact of the roughness Δz_{ins} on $G_\square$ is shown in Fig. 5 for $f_z = 1$ and $f_z = 0.01$. For these calculations, the amplitude of the original AFM data is numerically varied, and the Poisson problem is solved for every roughness Δz_{ins}.

As expected, the sheet conductance $G_\square$ decreases with the increasing surface roughness. Starting with a hypothetical perfect interface, the sheet conductance $G_\square$ drops to 25% for $\Delta z_{ins} \approx 7$ nm, which is equivalent to about two monolayers. Along a one-dimensional channel, this roughness would require frequent transfers with activation energies of several k_BT, and $G_\square$ would diminish drastically. Thus, the moderate decay of $G_\square$ with Δz_{ins} suggests that the macroscopic paths of the charge carriers rarely require thermal excitation. The cross sections of Fig. 2 reveal such conduction pathways over long distances. Consequently, the roughness of a two-dimensional channel has a reduced impact on the conductance $G_\square$. This notion is supported by conductance data obtained by setting $f_z = 0.01$ in order to simulate small transfer integrals between adjacent monolayers. Despite this severe reduction, we observe only a disproportionate decrease in less than 50% in sheet conductance even for a roughness of $\Delta z_{ins} \approx 7$ nm. Apparently, the vast majority of the inter-molecular charge transfers appear within the same monolayer.

The temperature dependence of the sheet conductance shown in Fig. 6 fits the understanding that charge carriers rarely have to hop between adjacent monolayers. With decreasing temperature T, the Fermi–Dirac distribution will further concentrate the charge carriers

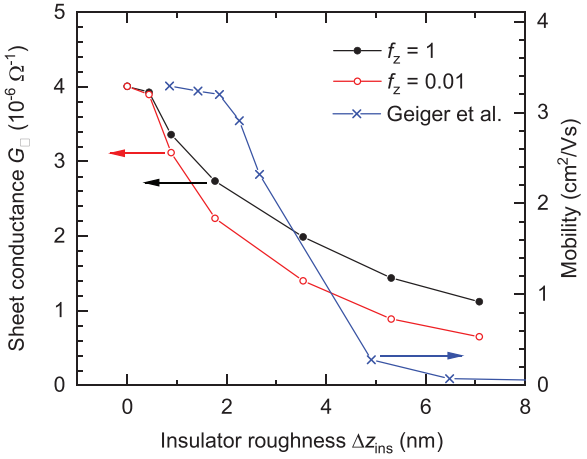

FIG. 5. Calculated sheet conductance $G_\square$ in dependence on the RMS roughness of the insulator at a lattice temperature of $T = 300$ K (dots and circles). The reduction of the interlayer conductance is considered by the factor f_z. The crosses show experimental data of Geiger *et al.*[12]

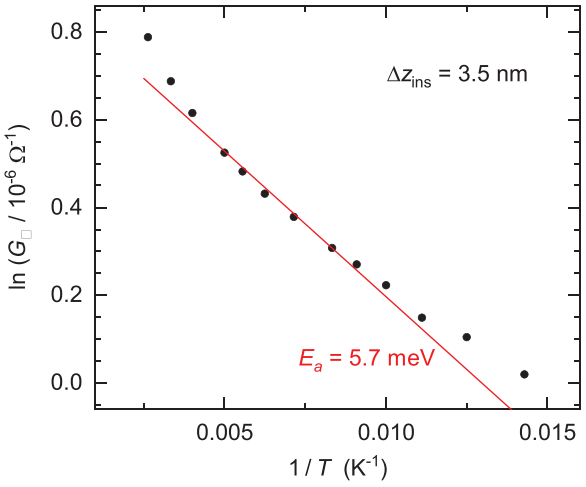

FIG. 6. Arrhenius plot illustrating the dependence of the sheet conductance $G_\square$ on temperature T for a roughness of $z_{ins} = 3.5$ nm and $f_z = 1$. The solid line fits the data with an activation energy of $E_a = 5.7$ meV.

within the first monolayer. Thermally activated transfers of about 70 meV between adjacent monolayers will become less probable. For such transfers, an exponential relation between sheet conductivity $G_\square$ and $1/T$ is expected. However, the sheet conductances deviate from such an Arrhenius type behavior as indicated by the line in Fig. 6. Moreover, such a fit would produce unrealistic small activation energies of about 5.7 meV. The deviation from Arrhenius behavior and the small activation energy support the understanding that charge carriers rarely have to overcome potential barriers on their way across two-dimensional channels. Such percolation pathways appear in Figs. 2(c) and 2(d) as extended areas with high carrier density. The cross sections of (c) and (d) are separated by one monolayer. Thus, within these areas, the charge carriers can be transported within the same monolayer over distances of several hundred nanometers.

The calculated data in Fig. 5 show qualitative agreement with the experimental data of Geiger *et al.*[12] obtained on field-effect transistors of dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) field-effect transistors. The authors report that as the roughness increases the DNTT grain sizes decrease. Thus, charge carriers frequently have to overcome grain boundaries, which reduces the device's mobility. The impact of grain boundaries was not considered in the present study. However, the comparison of calculated and experimental data suggests the following picture: At low surface roughness, the decrease in conductivity mainly results from surface roughness alone. With increasing roughness, the impact of grain boundaries takes over and drastically reduces sheet conductance within the channel region.

In conclusion, we accessed the impact of interface roughness on channel conductance in molecular field-effect devices. Experimental AFM data were merged with self-consistent calculations of local potentials and charge carrier distributions. The high concentration of charge carriers at the interface leads to strong Coulomb screening vertical to the layers, as well as within the plane of the interface. We found that an interface roughness of about one monolayer reduces sheet conductance by about 50%. This surprisingly moderate reduction can be

explained by conduction paths that rarely require charge transfers between the first monolayers of the organic semiconductor.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts of interest to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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